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**Digital Control Techniques for Efficiency Improvements in
Single-Phase Boost Power Factor Correction Rectifiers**

by

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Digital Control Techniques for Efficiency Improvements in Single-Phase Boost Power Factor
Correction Rectifiers
written by Fu-Zen Chen
has been approved for the Department of Electrical Computer and Energy Engineering

Prof. Dragan Maksimović

Dr. Luca Corradini

Date _____

The final copy of this thesis has been examined by the signatories, and we find that both the content and the form meet acceptable presentation standards of scholarly work in the above mentioned discipline.

Chen, Fu-Zen (Ph.D., Electrical Engineering)

Digital Control Techniques for Efficiency Improvements in Single-Phase Boost Power Factor Correction Rectifiers

Thesis directed by Prof. Dragan Maksimović

Input current shaping has been required in AC-DC rectifiers in order to comply with regulations that specify limits on input current harmonics. Boost power factor correction (PFC) rectifiers are widely used to achieve near-unity input power factor and low current harmonic distortion. This thesis addresses digital control techniques aimed at improving efficiency and reducing harmonic distortion in digitally controlled single-phase boost PFC rectifiers operating over wide range of loads. By taking advantage of the flexibility of digital controllers and using a discontinuous conduction mode (DCM) detection circuit, several proposed control techniques achieve low current harmonic distortion and improve system efficiency over wide load range in DCM and in continuous conduction mode (CCM). In heavy load operation, a simple passive power sharing technique is introduced for interleaved boost PFC rectifiers to increase system power modularity; in medium to light load operation, proposed adaptive approaches improve light load efficiency by extending switching period to achieve low voltage switching and by adjusting switching frequency to scale with processed power. Furthermore, a new current error estimation approach is applied to relieve current sensing limitations and to reduce current controller design effort. Digital control techniques are implemented and verified using field programmable gate array (FPGA) in several boost PFC rectifier prototypes.

Dedication

To my lovely family.

Acknowledgements

First, to my lovely wife Peiju, my parents and my sister Yiling; without their support and encouragement, none of this would have happened.

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Chapter 1

Introduction

Most electrical and electronics applications require DC power supplies. Nonetheless, utility systems usually generate, transmit and distribute power with constant frequency ac voltage. A rectifier is the power electronics interface that converts ac power to DC power. AC-DC rectifiers may supply DC power to different electrical loads, but they are all connected to the same ac line input. To maintain the quality of the ac line, standards and recommendations set current harmonics and power factor limitations on rectifiers in applications, such as computer power supplies. The AC-DC rectifier that achieves low current harmonics and a good power factor (close to 1) is called the power factor correction (PFC) rectifier.

As the front-end stage of most computer power supplies, PFC rectifiers are more in demand than ever with the progress of information technology. According to the U.S. Environmental Protection Agency, energy used by servers and data centers was 1.5 percent of total U.S. electricity consumption in 2006 and is expected to be higher in the future [1]. Environmental impact from computing power has been addressed recently [1–5]. In response to increasing energy cost and environmental concerns, various energy efficiency initiatives and programs are addressing power conversion efficiency and power quality in data centers and computer power supplies [6, 7]. For example, to qualify for the highest (“Platinum”) certification in the 80 Plus program addressing data center power supplies operating from 230 Vrms ac line, the power supply efficiency must exceed 91% at 100% load, 94% at 50% load, and 90% at 20% load, with power factor greater than 0.95 at 50% load [6]. It is expected that future energy efficiency program specifications will be even more

demanding in terms of efficiency, power factor and current harmonic distortion requirements for off-line power supplies over even wider load ranges.

Among the switched-mode PFC rectifiers, boost or buck-boost topologies are more popular due to their good current shaping ability over the entire ac line period. In general, boost PFC rectifiers have higher conversion efficiency than buck-boost PFC rectifiers, which makes boost topology the most popular structure for PFC rectifiers. In boost PFC rectifiers, although analog control circuits have successfully been applied for current shaping, with the rapid progress of digital processes, digital control circuits are becoming more attractive due to their potentials for improved flexibility, programmability, reduced sensitivity to noise, reduced component count, etc.

This thesis focuses on digital control techniques for efficiency improvements and reductions of current harmonic distortion over a wide range of loads in single-phase boost PFC rectifiers. An introduction to boost PFC controllers, including analog and digital controllers, is given in the first part of Chapter 2. Then, motivation for the work presented in this thesis is discussed, while the last part of Chapter 2 reviews existing boost PFC control approaches to deal with efficiency improvements and wide load range operation, both in continuous conduction mode (CCM) and in discontinuous conduction mode (DCM). In Chapter 3, an adaptive switching light load efficiency improvement approach is introduced. This approach includes a new current sensing correction factor and an adaptive switching technique to reduce current harmonic distortion and to reduce switching losses in DCM. Based on the adaptive CCM/DCM control, an adaptive frequency approach, which further improves light load efficiency, is introduced in Chapter 4. A current error estimation technique is introduced in Chapter 5 to replace the traditional analog to digital converter in inductor current sensing. Chapter 6 applies adaptive switching approaches and the passive power sharing technique in interleaved boost PFC rectifiers to enable system power modularity. Chapter 7 summarizes the original contributions and concludes this thesis.

Chapter 2

Review of Switched-Mode Power Factor Correction Rectifiers

This chapter provides a brief introduction to the existing controllers for boost power factor correction (PFC) rectifiers and describes the motivation for the research presented in this thesis. First, basic principles of the boost switched-mode power converter are described in Section 2.1, followed by an introduction to popular analog and digital boost PFC controllers in Section 2.2. Then, motivations for the research on efficiency improvement and wide load range operation are addressed in Section 2.3. Some issues related to the research targets, boost PFC rectifiers with efficiency improvement and over wide load range operation, are addressed in the last two sections in this chapter.

2.1 Boost Switched-Mode Power Converter

Boost converter is one of switched-mode power converters, as illustrated in Fig. 2.1. For the switched-mode power converters, one common modulation is the pulse width modulation (PWM). PWM converters regulate voltage or current by adjusting the duty ratio (d) of the transistor gate control signal (g) with a constant switching frequency (f_s). During dT_s interval, g is logic high and transistor (Q) conducts, which pulls the switch node voltage (v_{ds}) low. Voltage across inductor (L) is positive and ramps the inductor current (i_L) up. At the end of dT_s , Q is turned-off and i_L flows through the diode (D). During the diode conduction interval, voltage across the inductor is negative, which makes i_L ramp down. If diode D conducts over the rest of the switching period (T_s), which means that i_L stays positive, the converter is operated in continuous conduction mode

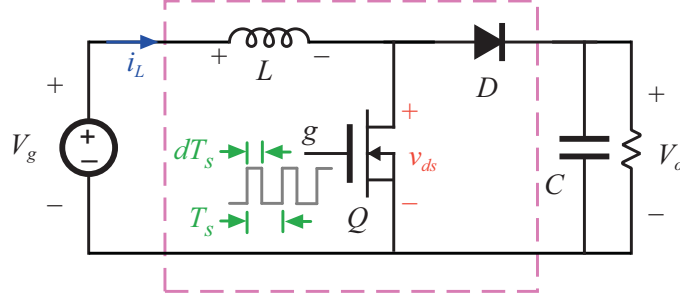


Figure 2.1: DC-DC boost converter circuits.

(CCM). CCM waveforms are illustrated in Fig. 2.2(a). On the other hand, if i_L ramps down to zero before the end of T_s , the converter is in discontinuous conduction mode (DCM), as shown in Fig. 2.2(b). CCM and DCM differ in dynamics, which affects controller design and bandwidth of the regulation loop.

2.2 Boost Power Factor Correction Controllers

Single-phase low-harmonic PFC rectifiers are usually the front-ends of electronic power supplies. The PFC rectifier is an AC-DC rectifier that achieves low input current harmonics and a good power factor (PF). The ideal PFC rectifier has the PF equal to 1 and has zero total harmonic distortion (THD) for a sinusoidal ac input. PF is defined as the ratio between the real power transmitted to the load and the apparent power from the source, as

$$\text{PF} = \frac{\text{average power}}{(\text{rms voltage})(\text{rms current})}. \quad (2.1)$$

THD of the ac current signal is defined as

$$\text{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1}, \quad (2.2)$$

where I_n is the magnitude of the n^{th} current harmonic.

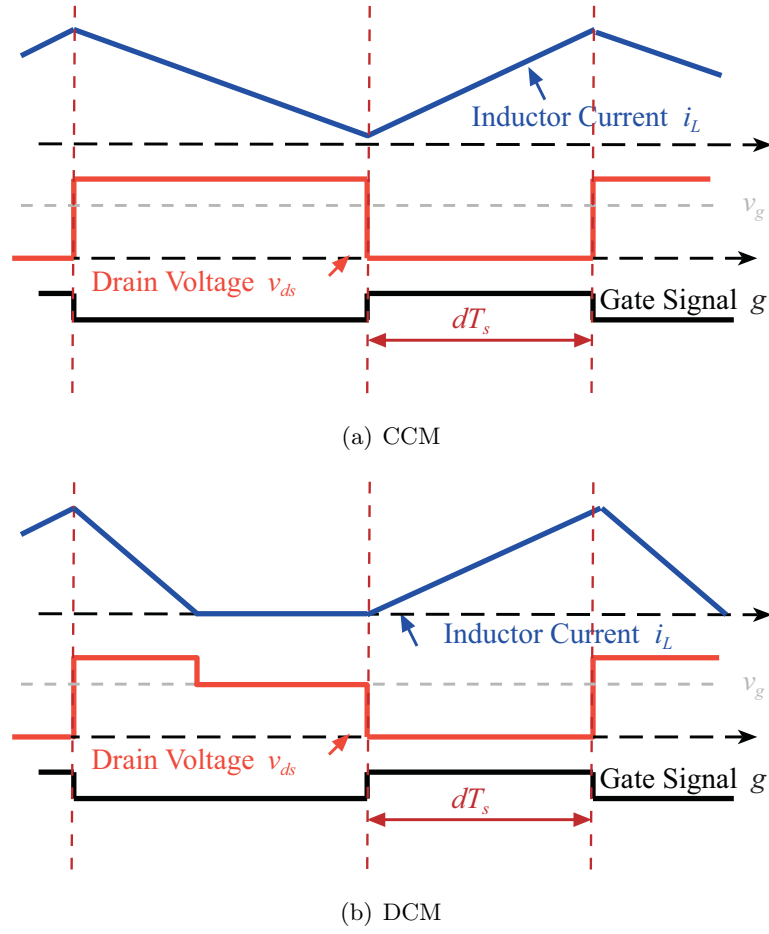
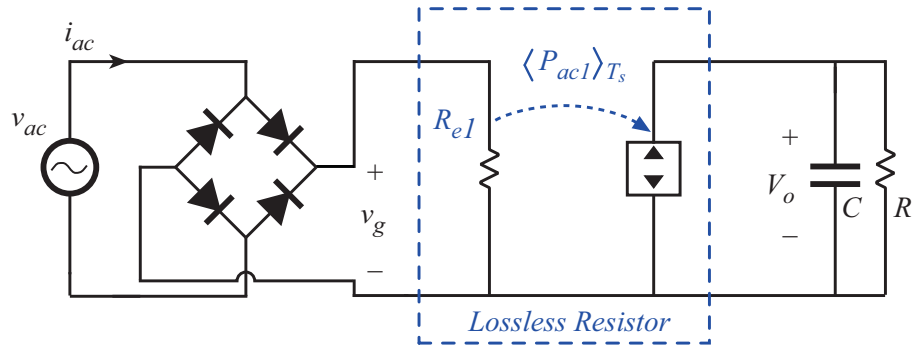


Figure 2.2: Boost converter waveforms in CCM and DCM, including inductor current i_L , switching node voltage v_{ds} , and gate control signal g .



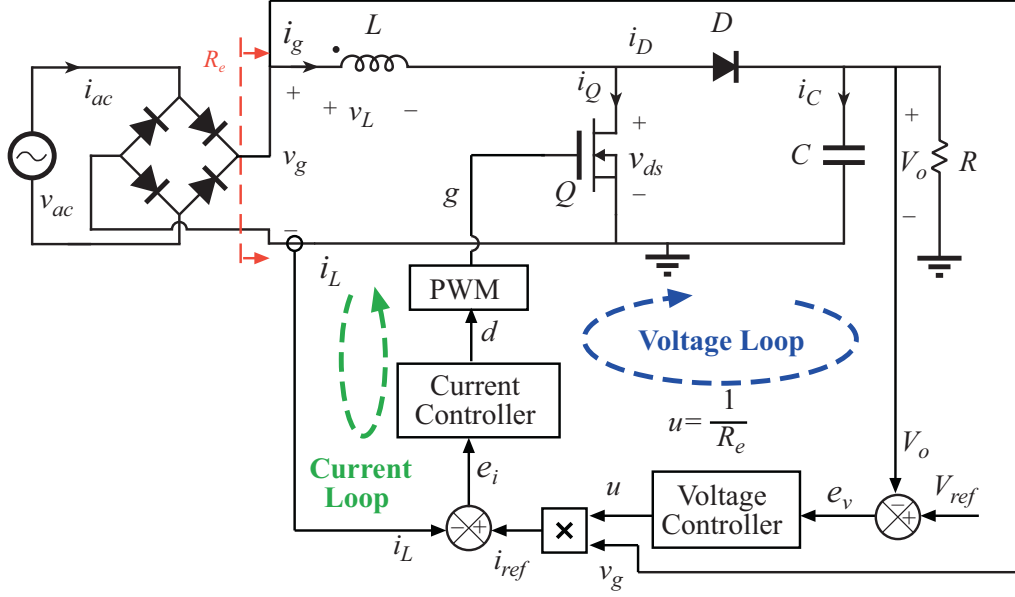


Figure 2.4: Block diagram of average current mode controller (boost example).

The input impedance of an ideal PFC rectifier at line frequency can be regarded as a loss-free emulated resistance (R_e), which transfers power to the output, as the model shows in Fig. 2.3 [8].

In this section, common approaches to control boost PFC rectifiers are shown and classified into two categories, analog controllers and digital controllers.

2.2.1 Analog Power Boost Factor Correction Rectifier Controllers

There are mainly three different types of the analog controllers in boost PFC rectifiers. These include average current mode controllers (ACM), critical conduction mode controllers, and charge controllers, such as nonlinear carrier controllers (NLC).

ACM has both current loop and voltage loop, as shown in Fig. 2.4 [8]. The voltage loop regulates the output voltage (V_o) and generates the power control command (u), which multiplies the rectified input voltage (v_g) to generate the reference current (i_{ref}). Current controller regulates inductor current (i_L) to follow i_{ref} , and achieves resistive load (R_e) to the ac input. The ACM approach needs a multiplier to generate the reference current; therefore, it is considered a multiplication approach.

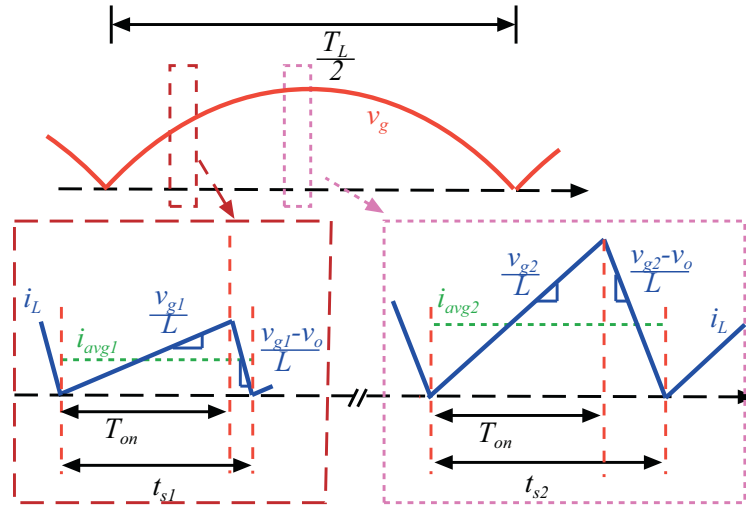


Figure 2.5: Operation waveforms of critical conduction mode control (boost example).

Critical conduction mode controller, also called transition mode (TM) controller, operates the boost PFC rectifier at the boundary between CCM and DCM, as the waveforms show in Fig. 2.5 [8]. Critical conduction mode controller keeps a fixed transistor turn-on interval (T_{on}) over half of the line period (T_L) and ends the transistor turn-off interval when the inductor current (i_L) reaches zero. Therefore, the switching period (T_s) varies over T_L . Critical conduction mode controller makes the average inductor current (i_{avg}) follow the input voltage and exhibits loss-free-resistor (R_e) as

$$R_e = \frac{v_{g1}}{i_{avg1}} = \frac{v_{g2}}{i_{avg2}} = \frac{2L}{T_{on}}, \quad (2.3)$$

without the need for reference current multiplication. Critical conduction mode boost PFC controllers are classified as the voltage follower type.

The third approach is nonlinear carrier control (NLC). NLC controller applies the ideal quasi-steady state conversion characteristic in CCM and shapes the input current without input voltage sensing [9, 10]. NLC forms a simple current loop by using an integrator with reset and a Set-Reset flip-flop with a nonlinear carrier waveform generator, as illustrated in Fig. 2.6. When the amount of charge through the inductor (v_Q) reaches the nonlinear carrier waveform (v_C), the gate signal resets, as

$$v_Q(DT_s) = \int_0^{DT_s} i_L(\tau) d\tau = \frac{V_o \cdot T_s}{R_e} (D)(1 - D), \quad (2.4)$$

with corresponding waveforms shown in Fig. 2.7. The advantages of NLC are that it requires no input voltage sensing or multiplication, and current compensator design requirements are reduced.

In addition to the analog PFC controllers mentioned above, digital PFC controllers are getting more and more attention. An overview of some recently developed digital PFC controllers is given in the next section.

2.2.2 Digital Power Factor Correction Rectifier Controllers

Early developments of digitally controlled boost PFC rectifiers involved control algorithms suitable for digital signal processors (DSP) and control algorithms with extra features, such as improving the voltage loop dynamic response [11–16]. Predictive current control (PCC) is one of the DSP suitable control algorithms. Different from the digital average current mode control, PCC applies predictive rules to simplify the digital current loop design. The simplest predictive control rule is equivalent to adding a duty ratio feed-forward term in the digital average current feedback controller to reduce current distortion [17–21]. Some sensorless approaches take advantage of the flexibility of the digital controller and then estimate or predict the other parameters. Input voltage estimation approach, inductor current rebuilt approach and digital nonlinear carrier approach have been developed. The input voltage estimation approach estimates the input voltage using disturbance observers [22]. The input current rebuilt approach estimates the inductor current based on the input/output voltages and the transistor on/off intervals [23]. The digital nonlinear carrier approach uses the quasi-steady state relationship between input and output voltages to calculate the required duty ratio [24]. In addition, digital control can also be applied in DCM by calculating the duty ratio appropriately [25].

2.3 Research Motivations

Efficiency is always the first consideration for power supplies. With the increase of energy prices, high efficiency power supplies gain more and more attention. Demanding high efficiency power supplies is based not only on economic reasons but is also based on environment protection considerations. With the explosion of the information technology, the environmental impact of computer power supplies has been considered and addressed [1, 2].

Nowadays, power supply companies have started to shift their focus from heavy load efficiency to high efficiency over a wide load range. Electronic systems are not always operated at the rated power; they are also operated at light load, in sleep mode, or in stand-by mode. In regular

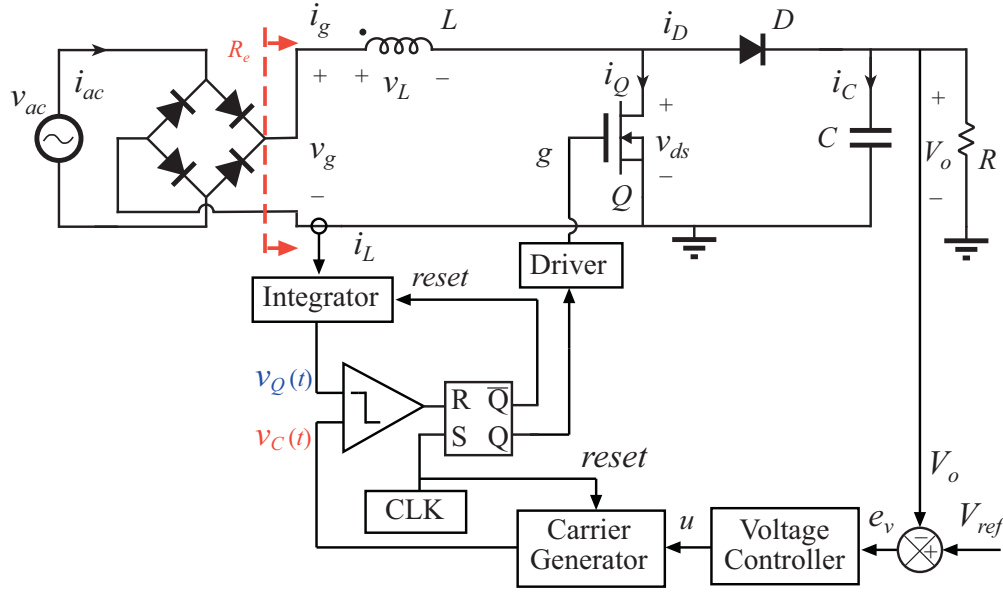


Figure 2.6: Block diagram of nonlinear carrier controller (boost example).

power supplies, efficiency drops dramatically at light load [26]. From an energy loss point-of-view, this is equivalent to having low efficiency. Therefore, energy standards have started to set the efficiency criteria across the whole range of the load conditions [6, 7]. The 80plus program launched specifications for power supplies in 2004, as 80% efficiency at 20%, 50%, 100% rated power [6]. Today, all computer power supplies have to pass the 80plus standard in order to obtain an Energy Star certificate [7].

As the front-end of power supplies, power factor correction rectifier is the main block to achieve high power factor and to maintain the low line current harmonic distortion. In order to maintain grid network quality, most of the consumer electronic devices rated from 75W to 1kW are required to meet the low-frequency harmonics limits of the European standard (EN61000-3-2), adopted in 2001. For the power factor limitation, computer power supplies have to meet 0.9 PF at the 100% rated power to be certified by Energy Star. Some applications, such as lighting applications, have different standards [7].

Furthermore, since 2007, Climate Saver Computing Initiative (CSCI) and other initiatives have aimed to set stricter standards, including using rating levels of bronze, silver, gold, and

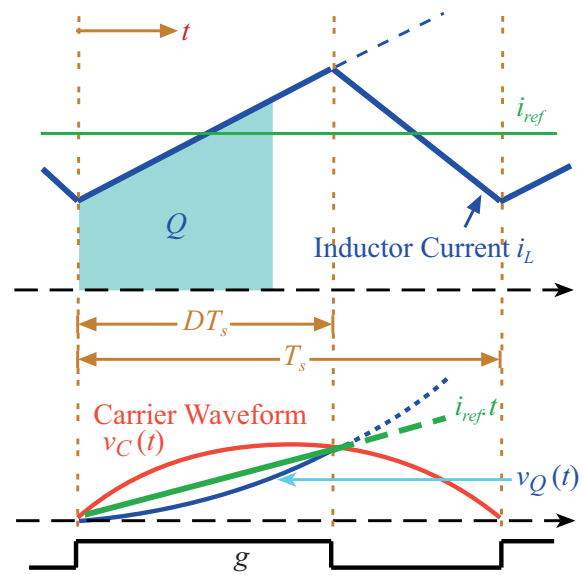


Figure 2.7: Operation waveforms of nonlinear carrier control (boost example).

Rated Power	Bronze	Sliver	Gold	Platinum
η at 20% load	82%	85%	87%	–
η at 50% load	85%	88%	85%	–
η at 100% load	82%	85%	87%	–
PF at 20% load	0.8	0.8	0.8	–
PF at 50% load	0.9	0.9	0.9	–
PF at 100% load	0.95	0.95	0.95	–

Table 2.1: Climate Savers Computing specifications for multi-output power supply units (η : efficiency, PF: power factor).

platinum levels, which not only push the efficiency limitation to be higher over wide load range, but also change the power factor requirement from full load to medium load range [6]. The highest performance requirements for data center applications, are set for the platinum level: at 20%, 50%, 100% of the rated load, minimum efficiencies are 90%, 94% and 91%, with 0.9 power factor at 50% rated power (Table 2.1 and Table 2.2) [2, 6]. It is believed that in the near future, both the efficiency limitation and the current harmonics standard are going to be stricter and be applied to even lower power levels.

Due to the high efficiency and the low current harmonics requirements of the PFC rectifiers over a wide range of loads, a study of the boost PFC control approaches for reducing current harmonic distortion and improving the efficiency over wide load range is presented in this thesis. The issues related to the wide load operated boost PFC rectifiers are discussed in the next section, followed by the issues of the efficiency improvement in the boost PFC rectifiers.

2.4 Issues in Wide Load Operated Boost PFC Rectifiers

Among the controllers shown in Section 2.2 for the single-phase boost PFC rectifiers, the voltage follower approaches work as resistance emulators by operating the converter at DCM or boundary between CCM and DCM; multiplier approaches shape the input current to track the reference current with current mode regulation, such as ACM; NLC takes advantage of the CCM quasi-steady-state relationship to emulate input resistance without input voltage sensing. Most of

Rated Power	Bronze	Sliver	Gold	Platinum
η at 10% load	–	75%	80%	82%
η at 20% load	81%	85%	88%	90%
η at 50% load	85%	89%	92%	94%
η at 100% load	81%	85%	88%	91%
PF at 10% load	–	0.65	0.65	0.65
PF at 20% load	–	0.8	0.8	0.8
PF at 50% load	–	0.9	0.9	0.9
PF at 100% load	0.9	0.95	0.95	0.95

Table 2.2: Climate Savers Computing specifications for single-output power supply units (η : efficiency, PF: power factor).

the boost PFC controllers tend to operate in a limited load range in order to keep the power stage operating in the desired mode, CCM, DCM, or boundary between CCM and DCM.

The approaches intended for CCM operation can also run in DCM but with increased current harmonic distortion. In order to operate in CCM over a wide range of loads, there are two approaches that can be utilized. One is to increase the inductance value (L); the other is to increase the switching frequency (f_s). Increasing the inductance value not only slows the system dynamics but also increases the size and the cost of the inductor. Increasing the switching frequency introduces more switching loss, which results in poor efficiency especially at light load.

In the approaches intended for DCM operation or boundary between CCM and DCM operation, current sense is not necessary for input current shaping. As a result, they cannot be operated in CCM. Under CCM/DCM boundary operation, critical conduction mode PFC rectifiers change the switching frequency a lot, which increases the size of the input filter. DCM PFC controllers have to be able to operate in DCM at the rated power. Therefore, the large current ripple increases the system power loss and the electromagnetic interference (EMI) at heavy load.

In order to have the high efficiency PFC rectifier over wide range of loads, PFC controller has to be able to operate in both modes, CCM and DCM. Some dual-mode approaches operate two different controllers in different modes. Besides, when boost PFC rectifiers operate in DCM, there is DCM current oscillation phenomena, which causes DCM current distortion. This section

discusses the issues related to wide load range operated boost PFC rectifiers, including dual-mode operation and DCM distortion.

2.4.1 Dual-Mode Operated Boost PFC Controllers

For getting the low current harmonic distortion, non-mixed-mode controller approaches keep the same operation mode over the entire ac line period (T_L). Non-mixed-mode PFC rectifiers always operate in one mode. CCM occurs over the entire T_L if

$$R_e \leq \frac{2L_{CCM}}{T_{s,CCM}}. \quad (2.5)$$

The boost PFC operates in DCM for the entire T_L at light load if

$$R_e \geq \frac{2L_{DCM}}{T_{s,DCM} \cdot \left(1 - \frac{V_M}{V_o}\right)}, \quad (2.6)$$

where V_M is the peak line voltage over the line period.

Two different non-mixed-mode approaches result in operating in single mode over the entire line period T_L . One is changing the switching frequency; the other is changing the equivalent inductance. An approach based on changing the equivalent inductance (L_{eq}) to control the PFC operation mode is presented in [27]. It separates the boost inductor into two and adds a switch leg between the two inductors, as shown in Fig. 2.8. At heavy load, while boost PFC operates in CCM, it uses a nonlinear carrier controller with both inductors in series. At light load, the switch leg shorts as a capacitor; part of the inductor (L_f) with the capacitor (C_f) leg forms a DC side input filter before the boost PFC power stage. Due to the reduction of the inductance value, boost PFC operates in DCM over the entire line period. In DCM, it still uses the nonlinear carrier controller with a modified carrier waveform. In addition, some core materials vary their permeability and their corresponding inductance values with different DC bias to achieve wide load range operation [28, 29].

The approach of changing the switching frequency is similar to the approach of changing the

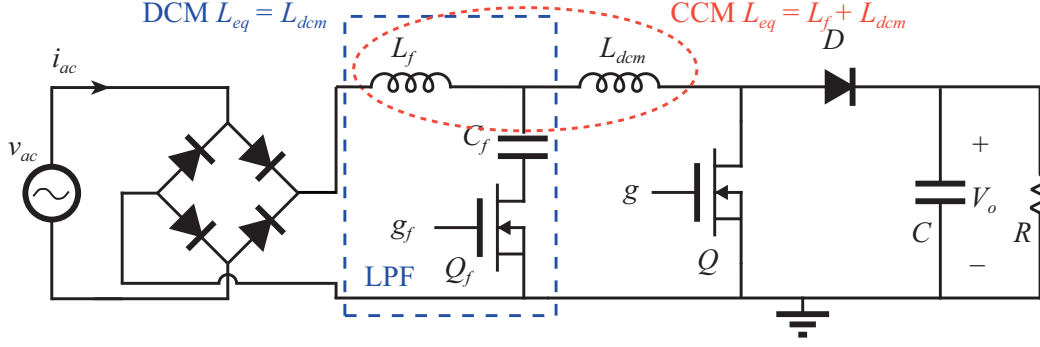


Figure 2.8: Dual mode boost PFC rectifier by changing L .

equivalent inductance value. It changes the switching frequency (f_s) to enforce the boost PFC rectifier to operate in one mode over the entire T_L [30]. The controller uses the predictive current control and calculates the required duty ratio for two different switching frequencies in either of the operating modes, CCM and DCM. Both approaches of changing the switching frequency and changing the equivalent inductor can operate over a wide range of loads and can reduce the current distortion due to the mode transition. However, non-mixed-mode PFC rectifiers have relatively large peak current in DCM and have low efficiency around the mode transition.

Dual-controller PFC rectifiers are able to operate in dual-mode within the ac line period. There are two approaches to changing the modes within T_L . One has constant on-time and variable frequency in both CCM and DCM [31]; while the other operates at a constant frequency in CCM and at varying frequency in DCM [32,33]. In CCM, the constant on-time approach uses the predictive valley current controller to calculate the off-time; while in DCM, it uses the estimated off-time without current sensing (Fig. 2.9). On the other hand, the constant frequency approach uses the digital average current mode control (DACM) in CCM [32,33]. When the boost power stage is in DCM, the constant frequency approach uses a semi-TM approach, which operates around CCM and DCM boundary with adding a constant charge-recovery interval as the discontinuous conduction period, as illustrated by the waveforms in Fig. 2.10. Constant on-time and semi-TM controllers achieve high switching frequency around input voltage zero-crossing when the converter processes less power. This results in reduced efficiency.

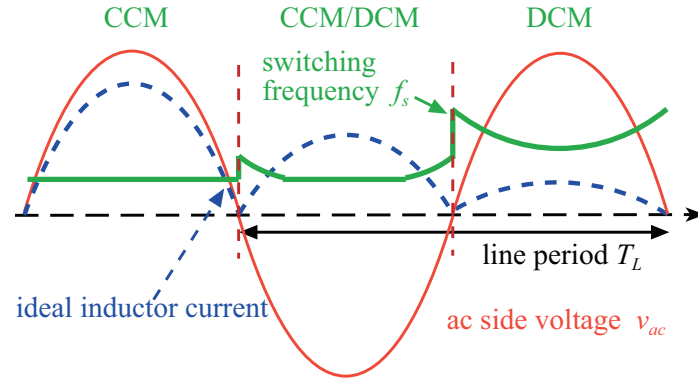


Figure 2.9: Operation waveforms illustrating constant on-time control in boost PFC rectifier.

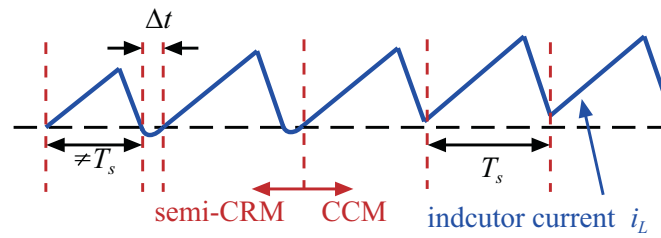


Figure 2.10: Inductor current waveform illustrates DACM + semi-TM operation.

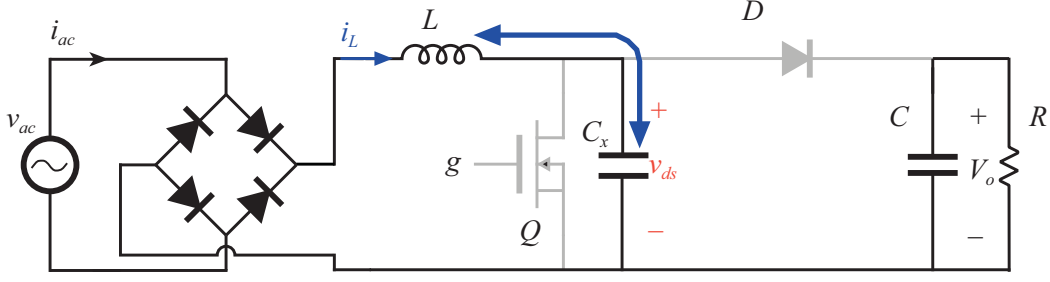


Figure 2.11: Boost PFC rectifier operated in DCM.

2.4.2 DCM Current Oscillation

When the boost PFC rectifier operates in DCM, there is a current oscillation phenomenon, DCM oscillation, which causes increased current distortion at light load. It has been studied and verified that DCM oscillation affects the current harmonic distortion when the boost PFC rectifier operates in DCM [34].

DCM oscillation happens during the discontinuous conduction interval (Fig. 2.11). During discontinuous conduction interval, inductor (L) and switch node capacitance (C_x) form a low-damping LC resonant tank, where energy bounces between L and C_x . The DCM oscillation starts from the time when the diode stops conducting and the switching node voltage (v_{ds}) equals to output voltage (V_o). Due to the voltage potential difference between rectified input voltage (v_g) and V_o , i_L rings around zero and v_{ds} rings around v_g . This is called the DCM oscillation.

For constant switching frequency operation ($f_s = 1/T_s$), the boost transistor may start to conduct at any v_{ds} in the discontinuous conduction interval (T_{dcm}) because of the DCM oscillation. Therefore, the inductor current level is not always zero at the time when the boost transistor starts to conduct, which affects the average current over T_s . Also, the switch node capacitance (C_x) is composed of inductor parasitic capacitance and semiconductor parasitic capacitance, including the transistor and the diode parasitic capacitance. Semiconductor parasitic capacitances are nonlinear capacitances which are affected by the voltage across the devices. Therefore, the constant frequency operated PFC rectifiers suffer from the DCM current distortion due to the DCM oscillation (Fig.

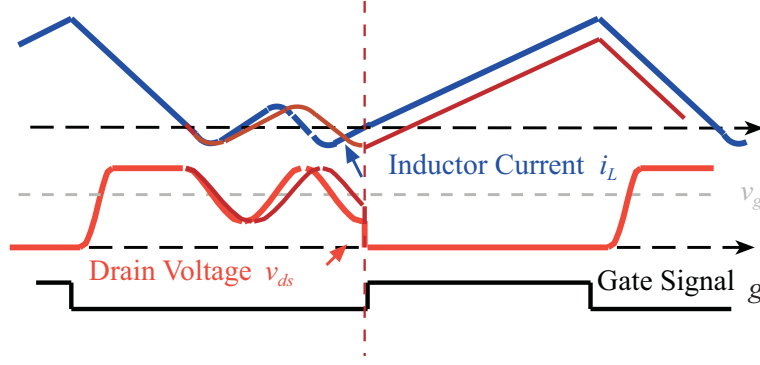


Figure 2.12: Waveforms illustrate DCM current distortion due to DCM oscillation (boost example).

2.12).

In order to reduce the current distortion due to the DCM oscillation, RC damping approaches have been studied in [34]. An RC snubber leg, consisting of a capacitance (C_{sn}) in series with a resistor (R_{sn}) at the switching node, is added as illustrated in Fig. 2.13. The RC damping approach successfully reduces the DCM oscillation and the DCM current distortion. However, the snubber leg, R_{sn} and C_{sn} , has to be a low impedance path to produce the damping effect. As a result, losses are increased and converter efficiency is reduced.

2.5 Efficiency Improvement in PFC Rectifiers

In the past few years, efficiency improvement approaches for the boost PFC rectifiers from component, control and topology aspects have been developed [35]. From the component point of view, silicon carbide (SiC) diode and the new structure of metal oxide silicon field effect transistor (MOSFET), CoolMOS, have reduced the PFC loss [36,37]. SiC diodes have less reverse-recovery charge than the regular silicon diodes. CoolMOSs have lower on-resistance than the regular vertical power MOS transistors; SiC diode and CoolMOS make transistor turn-on time shorter and reduce the transistor conduction loss. From the control point of view, paralleling modules with a shedding approach improves the light load efficiency but increases the number of components, as Fig. 2.14 shows [38–40]. Burst mode operation also helps to improve the light load efficiency, but also possibly generates audio noise [41]. Conduction angle control saves the switching loss but increases

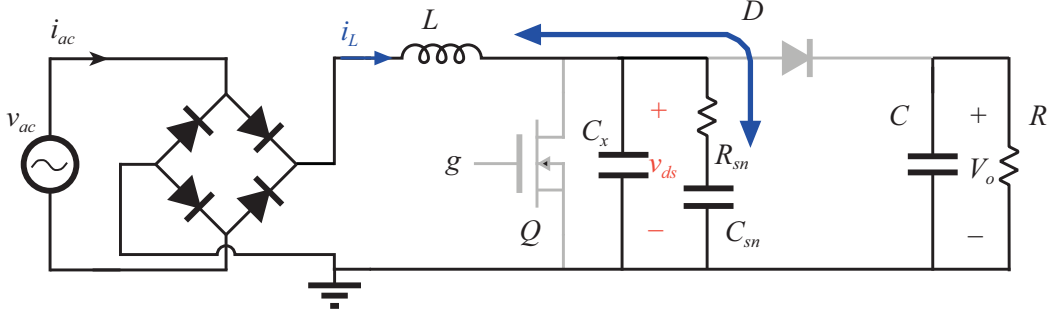


Figure 2.13: Boost PFC rectifier operated in DCM with RC damping snubber.

the current harmonic distortion by keeping the transistor turned-off around zero-crossings of the line input voltage (v_{ac}), as shown in Fig. 2.15 [42].

From the topology point of view, active snubber approaches to achieve zero voltage switching (ZVS) or zero current switching (ZCS) reduce reverse recovery loss of boost PFC rectifiers by adding extra components and increasing overall system complexity [43–45]. Bridgeless boost PFC rectifiers increase overall efficiency by eliminating the full bridge rectifier and eliminating one conduction loss component in the conduction path (Fig. 2.16) [35, 46, 47].

Among the various efficiency improvement approaches, some could be combined together. For the topology selection, in comparing the complexity of the system with the performance improvement, the regular boost PFC with full bridge rectifier approach is still the most attractive one. Recently, bridgeless boost PFC rectifiers and interleaved boost PFC rectifiers get more attention due to the heavy load efficiency improvement and improved system modularity. For the controller selection, a smart but complicated PFC controller is difficult to be embedded in the regular analog PFC controllers. A digital controller can easily add extra functions without increasing the cost much. Digital control becomes the first choice to design the smart boost PFC controller.

This study focuses on the use of digital control for high efficiency over wide load range in single-phase boost PFC rectifiers.

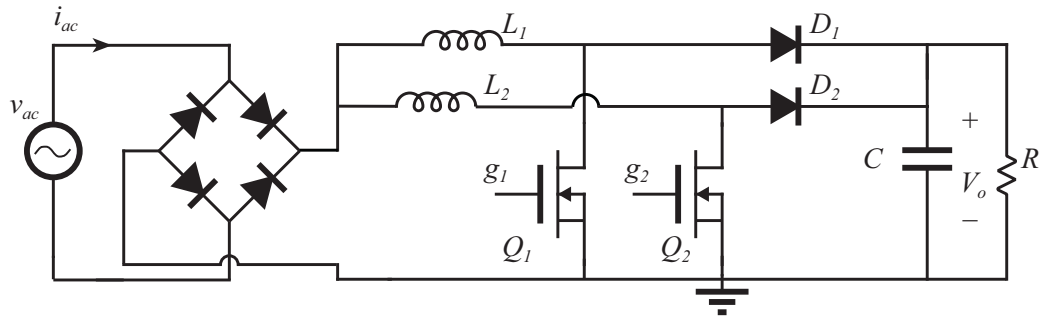


Figure 2.14: Multi-phase boost PFC rectifier.

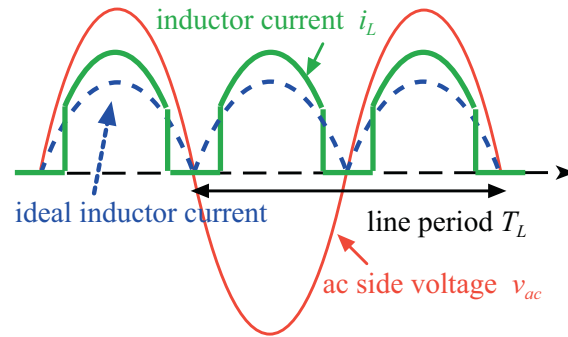


Figure 2.15: Waveforms illustrating conduction angle control in PFC rectifier.

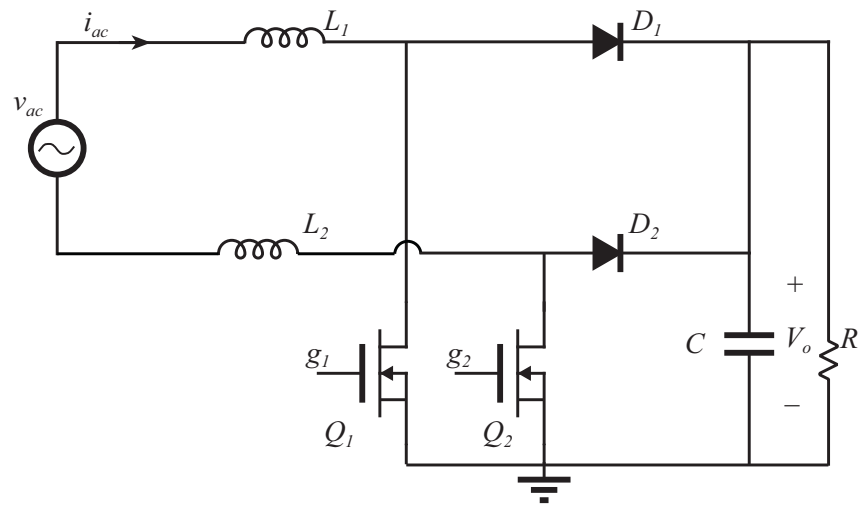


Figure 2.16: Bridgeless boost PFC rectifier.

Chapter 3

Adaptive Switching CCM/DCM Current Control in Boost PFC

Wide load range operated boost power factor correction (PFC) rectifiers require current shaping ability in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM). As mentioned in Chapter 2, most PFC controllers suffer from current harmonic distortion by operating in improper mode. Most of the dual-mode controllers have a discontinuity problem during mode transitions. In addition, boost DCM oscillation introduces current harmonic distortion when the converter is operating at light load in DCM. Although the RC damping approach relieves the current harmonic distortion, it reduces both the light load efficiency in DCM and heavy load efficiency in CCM [34].

In this chapter, a digital boost PFC controller that can operate over a wide range of loads with high efficiency is introduced. First, a review of the digital average current control (DACM) and the digital predictive current control (PCC), are discussed in Sec. 3.1. Then, a proposed approach, which corrects the digital current sensing error, is addressed. Sec. 3.2 introduces a new adaptive switching approach to reduce DCM current distortion without compromising system efficiency. A detail of the adaptive switching CCM/DCM current controller is presented in Sec. 3.3, followed by experimental results, including efficiency improvement and DCM current distortion reduction, in the last section.

3.1 Current Sampling Issue and Current Sensing Correction Factor

3.1.1 Digital Average Current Control / Predictive Current Control

DACM is one of the most popular control approaches in digitally controlled PFC rectifiers (Fig. 3.1). DACM senses output voltage (V_o) and passes the voltage error signal (e_v) through a voltage controller, which regulates the output voltage. Output of the voltage controller, power command (u), is multiplied with rectified input voltage (v_g) to generate current reference (i_{ref}). To reduce the current sampling rate, DACM controller senses the inductor current at the middle of the transistor conduction interval or diode conduction interval. The sensed current ($i_{L,sense}$) approximately represents the average inductor current over the entire switching period in CCM [17]. Current error (e_i), the difference between i_{ref} and $i_{L,sense}$, feeds into a current controller and a digital pulse width modulator (DPWM) to generate a gate control signal (g), which controls the boost transistor (Q).

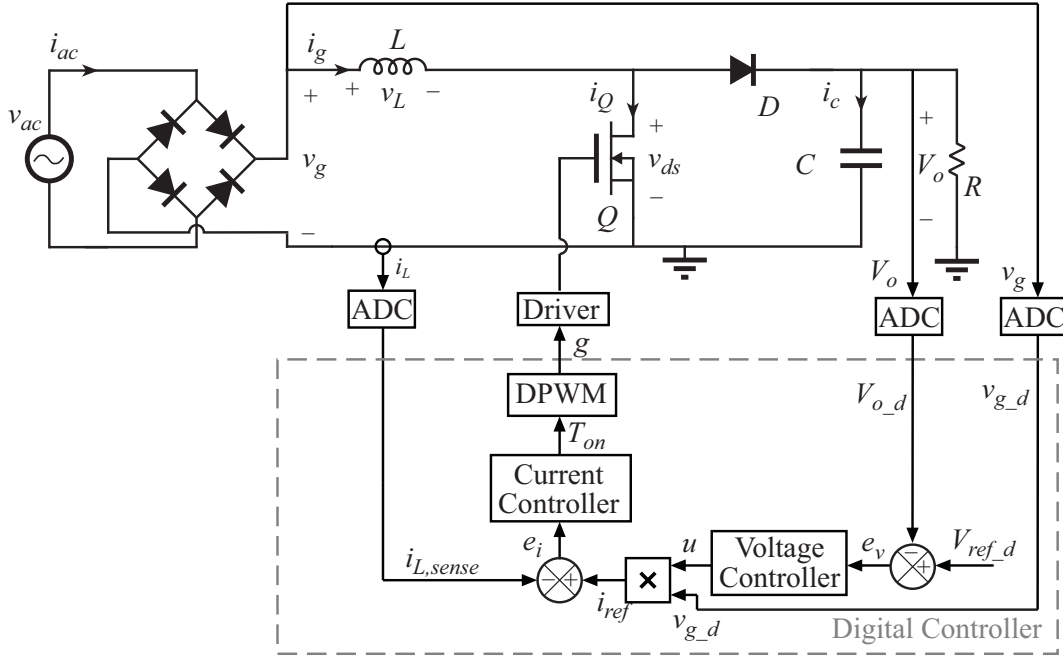


Figure 3.1: Block diagram of digital average current mode controller.

Predictive current control (PCC) technique is a high performance current control algorithm

with relatively simple digital implementation. Based on the low current sampling rate, PCC is a modification of DACM by using predictive rules. The next sensed inductor current value ($i_{L,sense}[n+1]$) can be expressed as a function of the previous sensed inductor current value ($i_{L,sense}[n]$), the controlled duty ratio ($d[n]$) and the operating conditions, as

$$i_{L,sense}[n+1] = i_{L,sense}[n] + \frac{v_g}{L} \cdot T_s - \frac{V_o}{L} \cdot T_s \cdot (1 - d[n]), \quad (3.1)$$

where d is the duty ratio; L is the boost inductor value; and $T_s = 1/f_s$ is the switching period.

By rewriting Eq. 3.1 and replacing $i_{L,sense}[n+1]$ with the desired sensed current i_{ref} , the required duty ratio ($d[n]$) to regulate inductor current can be calculated as

$$d[n] = \frac{L}{T_s V_o} \cdot (i_{ref} - i_{L,sense}[n]) + \left(1 - \frac{v_g}{V_o}\right). \quad (3.2)$$

Eq. 3.2 uses the inductor current relationship in a single cycle to calculate the duty ratio for the next switching period based on current error and input/output voltage information. Depending on the predictive rule, the inductor current error can be canceled out in the next switching period, or next few periods.

Some predictive rules use multiple cycles to calculate the required duty ratio [17], as

$$d[n] = \frac{L}{T_s V_o} \cdot (i_{ref} - i_{L,sense}[n]) + \left(1 - \frac{v_g}{V_o}\right) + \left(1 - \frac{v_g}{V_o}\right) - d[n-1]. \quad (3.3)$$

The current predictive rule can be considered as a modification of the digital average current mode control. Eq. 3.2 and Eq. 3.3 can be segmented into the digitally proportional current control rule plus a feed-forward term, which is the estimated steady state duty ratio in CCM.

From the small signal point of view, compared to the single cycle predictive rule (Eq. 3.2), the multiple-cycles predictive rule (Eq. 3.3) has an extra high frequency pole and increases the feed-forward gain. Ideally, the single cycle predictive rule reduces current error and regulates

inductor current in one cycle; while the multiple-cycle predictive rule takes multiple cycles (Fig. 3.2). However, multiple-cycle predictive rule also allows longer conversion time for current sensing.

3.1.2 Digital Current Sensing Error and Current Sensing Correction Factor

In DACM or in average PCC, the inductor current is usually sensed in the middle of the transistor conduction interval (T_{on}) or diode conduction interval (T_{off}). In CCM, the sensed current ($i_{L,sense}$) can represent the average current ($\langle i_L \rangle_{T_s}$) over the entire switching period (T_s), as shown in Fig. 3.3. However, in DCM, $i_{L,sense}$ no longer represents $\langle i_L \rangle_{T_s}$. The DCM current sensing error introduces some current distortion during light load operation.

To remove the current sensing error, a current sensing correction approach has been developed [48]. It introduces a current sensing correction factor (κ), which is the ratio between the sensed current ($i_{L,sense}$) and the average current $\langle i_L \rangle_{T_s}$. The current sensing correction factor proposed in [48] is based on estimation, as

$$\kappa = \frac{i_{L,avg}}{i_{L,sense}} = \sqrt{\frac{2L}{R_e T_s} \cdot \left(\frac{V_o}{V_o - v_g} \right)}. \quad (3.4)$$

Adding the current sensing correction factor in the controller successfully combines the CCM and DCM controllers as a single controller over wide load range. However, the estimated current sensing correction factor in Eq. 3.4 requires complicated calculation including a fast divider operation and a square root operation. Instead of using the estimation approach to calculate κ , a new approach, based on measurement, is introduced in this chapter. In DCM, the sensed current value only represents an average current value over the conduction interval, sum of the transistor conduction interval (T_{on}) and diode conduction interval (T_{off}) (Fig. 3.3). The conduction interval is the difference between T_s and discontinuous conduction interval (T_{dcm}). Therefore, the sensing based current sensing correction factor is

$$\kappa = \frac{i_{L,avg}}{i_{L,sense}} = \frac{T_{on} + T_{off}}{T_s} = 1 - \frac{T_{dcm}}{T_s}. \quad (3.5)$$

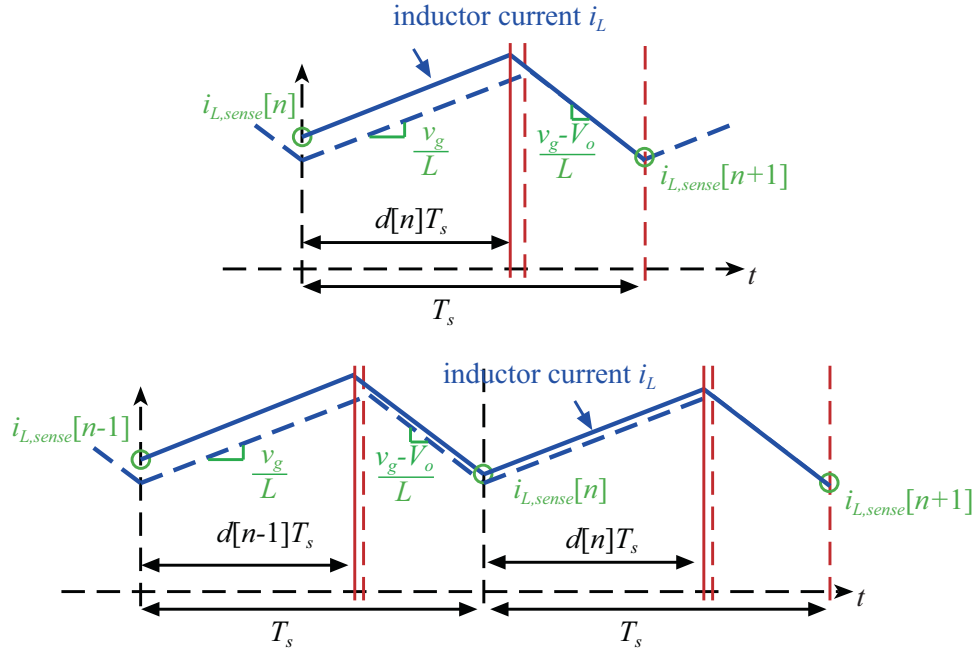


Figure 3.2: Single-cycle and multiple-cycle predictive rules.

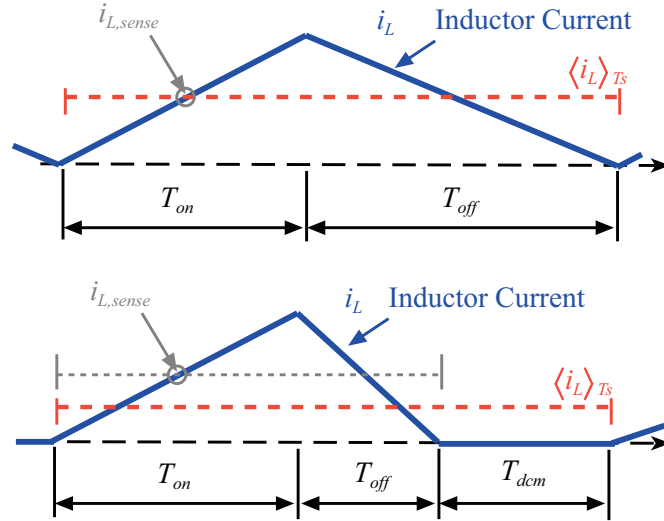


Figure 3.3: Current sensing in digital average current control under CCM (top) and DCM (bottom).

Instead of calculating the estimated value, this new approach detects T_{dcm} and uses a simple multiplication in the digital controller to correct the current sensing error.

Adding the current sensing correction term, the complete set of the CCM/DCM predictive current controller rules is as follows:

$$T_{on}[n+1] = \Delta T_{on}[n] + T_{on,ff}, \quad (3.6)$$

$$\Delta T_{on}[n] = \alpha \cdot e_i[n] + \alpha \cdot \beta \cdot e_i[n-1] + \Delta T_{on}[n-1], \quad (3.7)$$

$$e_i[n] = T_s[n] \cdot i_{ref} - (T_s[n] - T_{dcm}[n]) \cdot i_{L,sense}, \quad (3.8)$$

$$T_{on,ff} = \min \left[T_s \cdot \left(1 - \frac{v_g}{V_o} \right), T_s \cdot \sqrt{\left(1 - \frac{v_g}{V_o} \right) \cdot \frac{2Lu}{T_s}} \right], \quad (3.9)$$

where α is the term related to the current feedback gain; β is related to the zero location of the proportional and integral (PI) current feedback compensator; and $T_{on,ff}$ is the feed-forward term from PCC.

From the stability point of view, κ is always equal to 1 in CCM. Current loop stability in CCM is exactly the same as the regular average predictive current controller [17]. In DCM, for the estimation approach (Eq. 3.4), the current loop stability of current sensing correction approach in current loop has been addressed in [48]. However, since the proposed current controller has current sensing correction factor feedback, the block diagram of the current control loop can be constructed as shown in Fig. 3.4.

In addition to the current feedback loop, there is an extra κ feedback loop. Applying κ in Eq. 3.2 and correcting the duty ratio feed-forward in DCM (D_{ff}) as Eq. 3.10 and Eq. 3.11, small signal discrete transfer functions in z domain can be expressed:

$$d[n] = \frac{L}{T_s V_o} \cdot (i_{ref} - \kappa \cdot i_{L,sense}[n]) + D_{ff}, \quad (3.10)$$

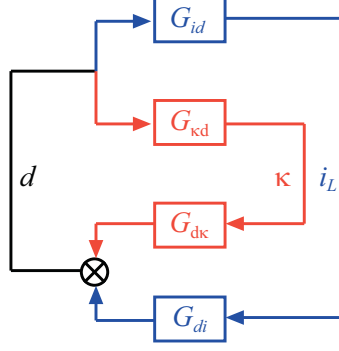


Figure 3.4: Block diagram of current loop with measured current sensing correction factor (κ).

$$D_{ff} = \min \left[\left(1 - \frac{v_g}{V_o} \right), \sqrt{\frac{2L}{R_e T_s} \cdot \left(1 - \frac{v_g}{V_o} \right)} \right], \quad (3.11)$$

$$G_{\kappa d}(z) = \frac{\hat{\kappa}}{\hat{d}} = \frac{V_o}{V_o - v_g}, \quad (3.12)$$

$$G_{d\kappa}(z) = \frac{\hat{d}}{\hat{\kappa}} = \frac{L \cdot i_{l,sense}}{V_o T_s} \cdot \frac{1}{z}, \quad (3.13)$$

$$T_{\kappa}(z) = \frac{1}{2} \sqrt{\frac{2L}{R_e T_s} \cdot \left(\frac{V_o}{V_o - v_g} \right)} \cdot \frac{1}{z}, \quad (3.14)$$

where T_{κ} is the κ loop gain. The κ loop has a gain always lower than 1, and the feedback loop is stable.

There are several ways to detect T_{dcm} . One simple way is to detect inductor current zero-crossing by a comparator and a digital controller to count T_{dcm} . This T_{dcm} detection approach is shown in the next section.

3.2 DCM Oscillation and Adaptive Switching

3.2.1 DCM Switch Approach and DCM Comparator

As mentioned in Chapter 2, DCM oscillation is one of the issues that causes current harmonic distortion at light load. Damping approach has been developed using an RC snubber leg to damp

out DCM oscillation [34]. RC damping approach reduces the current harmonic distortion in DCM, but it increases the snubber loss in both CCM and DCM. Instead of using the RC snubber leg, a new approach to reduce current distortion due to DCM oscillation is proposed and developed in this section.

The main idea is to store the DCM oscillation energy (E_{C_x}) from switching node capacitance (C_x) to inductor. The DCM oscillation energy stored in C_x is

$$E_{C_x} = \int_0^{V_o} C_x(v_{ds}) \cdot v_{ds} dv_{ds}. \quad (3.15)$$

A comparator and a switch (Q_{DCM}) across the secondary winding of the inductor are added, as shown in Fig. 3.5. During T_{dcm} interval, when the switching node voltage (v_{ds}) rings to be equal to the rectified input voltage (v_g), the controller sets the gate signal of the DCM switch (g_{DCM}) high to store the oscillation energy in the magnetizing inductance (L_M) and circulates current through Q_{DCM} . In order to find the correct timing to turn Q_{DCM} on, a DCM comparator is added across the inductor secondary winding to detect the inductor voltage (v_L) polarity. This comparator signal (s_{DCM}) also helps to detect CCM/DCM boundary and to measure T_{dcm} , as shown in Fig. 3.6. T_{dcm} information can be applied in Eq. 3.5, to correct the current sensing error and to reduce current harmonic distortion in DCM.

When boost transistor is turned on, energy stored in C_x is discharged immediately. Adding some dead-time (T_D) between boost gate signal (g) and DCM gate signal (g_{DCM}) saves energy (E_{save}), which depends on v_g , as

$$E_{save} = \min \left[\int_0^{V_o} C_x(v_{ds}) \cdot v_{ds} dv_{ds}, 2 \left(\int_{v_g}^{V_o} C_x(v_{ds}) \cdot v_{ds} dv_{ds} \right) \right]. \quad (3.16)$$

Ideally, DCM switch approach can recover most DCM oscillation energy in the boost PFC rectifier. However, the DCM switch has to be implemented using semiconductor switches, transistors and diodes. The DCM switch has to be able to block positive and negative voltages, and to allow current flow in one direction. Non-ideality of the DCM switch, forward voltage on the

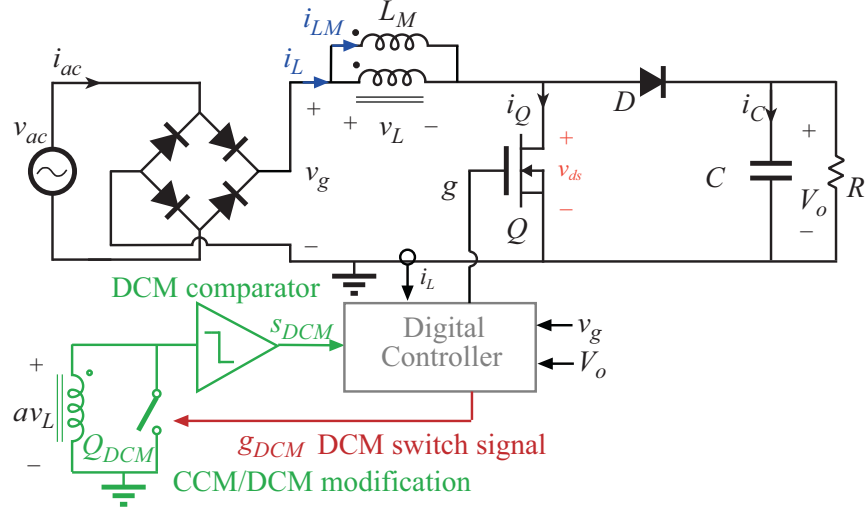


Figure 3.5: Block diagram of a boost PFC rectifier using the DCM switch.

diode and on-resistance of the transistor, reduces the saved energy (detailed analysis is shown in Appendix A). In addition, due to the non-ideality of the DCM switch, some parasitic capacitance exists. This is equivalent to adding extra capacitance at the switching node. Therefore, although the DCM switch approach reduces the input current harmonic distortion due to the DCM oscillation, its losses diminish efficiency improvements. Experimental results and waveforms are shown in Appendix A.

3.2.2 Adaptive Switching Approach

Due to the non-ideality of the DCM switch, the approach becomes one of the damping approaches. For high efficiency at light load, an adaptive switching approach is introduced in this section. The input current distortion due to the DCM oscillation is mainly caused by the uncertainty of the inductor current level when the boost transistor starts to conduct. If the transistor is always turned on at zero inductor current, the DCM current distortion will be reduced, as illustrated in Fig. 3.7. Therefore, the main idea of the adaptive switching approach is to adjust the turn-on timing of the boost transistor to meet zero inductor current condition. On the other hand, there are two zero inductor current conditions during DCM oscillation. One is at high switching node

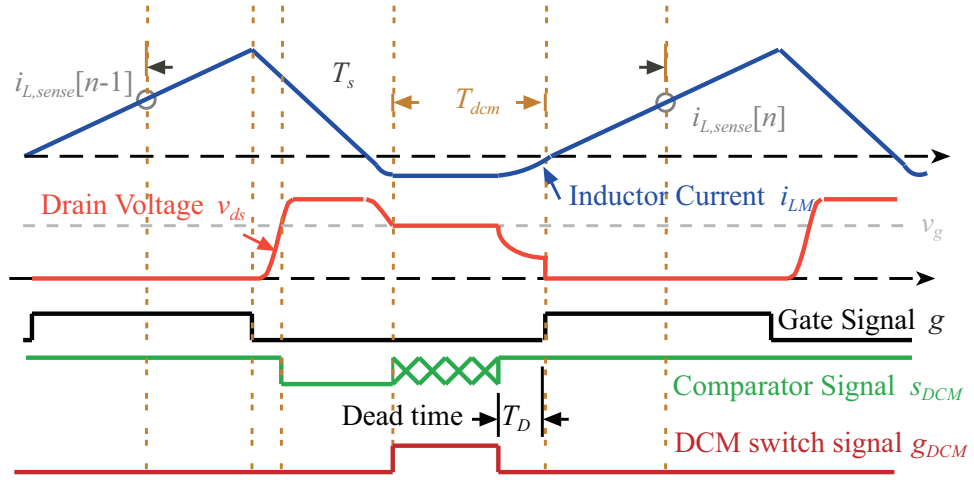


Figure 3.6: Operation waveforms illustrating the DCM switch approach.

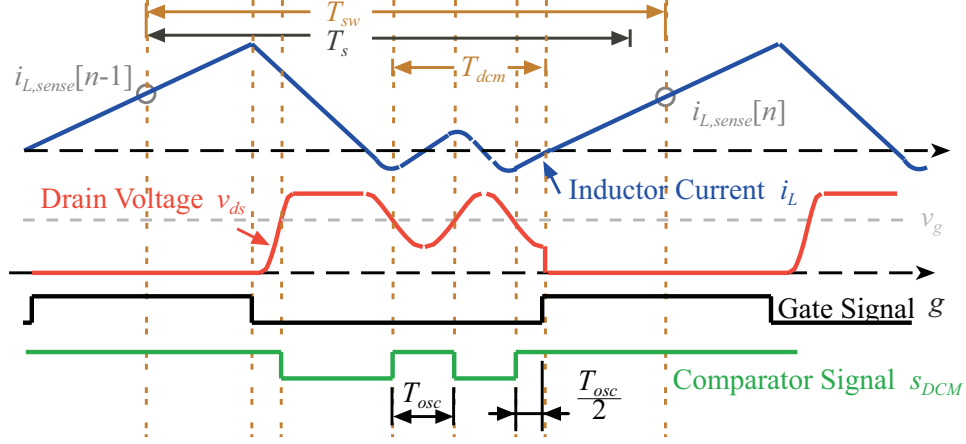


Figure 3.7: Operation waveforms illustrating adaptive switching approach.

voltage, while the other is at low switching node voltage, as shown in Fig. 3.7. If the boost transistor turns on at low switching node voltage, it saves the most switching node energy without adding extra active snubber circuits (Eq. 3.16).

In order to turn the boost transistor on at the lowest switching node voltage, DCM oscillation information is required. In DC-DC applications, since the input voltage is roughly a constant value, the DCM oscillation period can be considered constant. A simple RC delay can be applied to turn the boost transistor on at low switching node voltage [49–51]. RC delay approach has been applied to AC-DC rectifiers in transition mode (TM) to approximately achieve low voltage switching [32,33, 51]. However, DCM oscillation period changes a lot with different components and operating points in boost PFC rectifiers. Instead of applying the estimated delay time for low voltage switching, the proposed adaptive switching approach uses DCM comparator signal (s_{DCM}) to precisely measure part of the DCM oscillation period (T_{osc}) (Fig. 3.7). Taking advantages of digital control, the controller applies half T_{osc} after the rising edge of s_{DCM} to make the transistor turn-on at the lowest switching node voltage. The hardware implementation of the adaptive switching approach is a simple secondary winding of the inductor with a DCM comparator, as shown in Fig. 3.8.

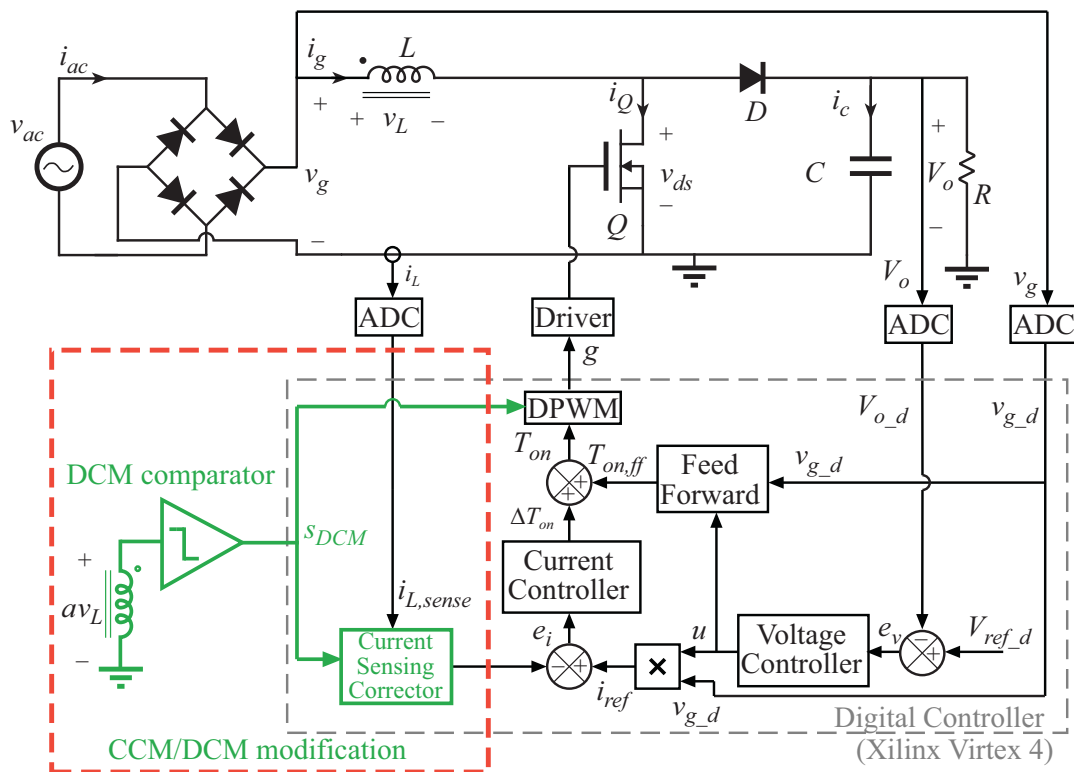


Figure 3.8: System block diagram for adaptive switching current controller.

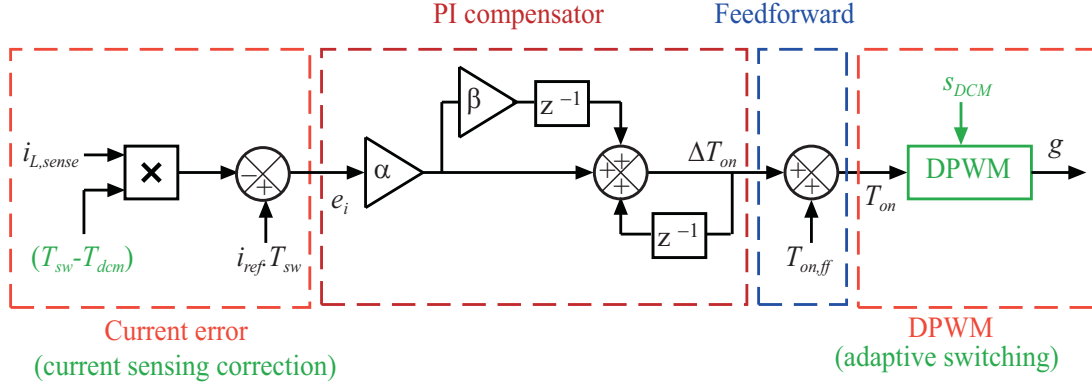


Figure 3.9: Block diagram of current controller (adaptive switching CCM/DCM control).

3.3 Adaptive Switching CCM/DCM Current Control

Adaptive switching CCM/DCM control combines the two proposed approaches described in previous sections, the new current sensing correction factor and the adaptive switching approach. Adaptive switching CCM/DCM control is based on the predictive current control with trailing triangle modulation and uses PI compensator for current loop (Eq. 3.2). The block diagrams are shown in Fig. 3.8 and Fig. 3.9. On the other hand, since the adaptive switching approach slightly changes the switching period, its control rule is modified from the constant frequency predictive rule. Instead of using a constant switching period (T_s), the adaptive switching CCM/DCM controller uses the measured switching period (T_{sw}) to calculate the current sensing correction term (Eq. 3.8). The modification affects the current compensator gain and zero location only (Eq. 3.7).

The complete set of the adaptive switching CCM/DCM predictive current control law is listed in the following equations:

$$T_{on}[n+1] = \Delta T_{on}[n] + T_{on,ff}, \quad (3.17)$$

$$\Delta T_{on}[n] = \alpha \cdot e_i[n] + \alpha \cdot \beta \cdot e_i[n-1] + \Delta T_{on}[n-1], \quad (3.18)$$

$$e_i[n] = T_{sw}[n] \cdot i_{ref} - (T_{sw}[n] - T_{dcm}[n]) \cdot i_{L,sense}, \quad (3.19)$$

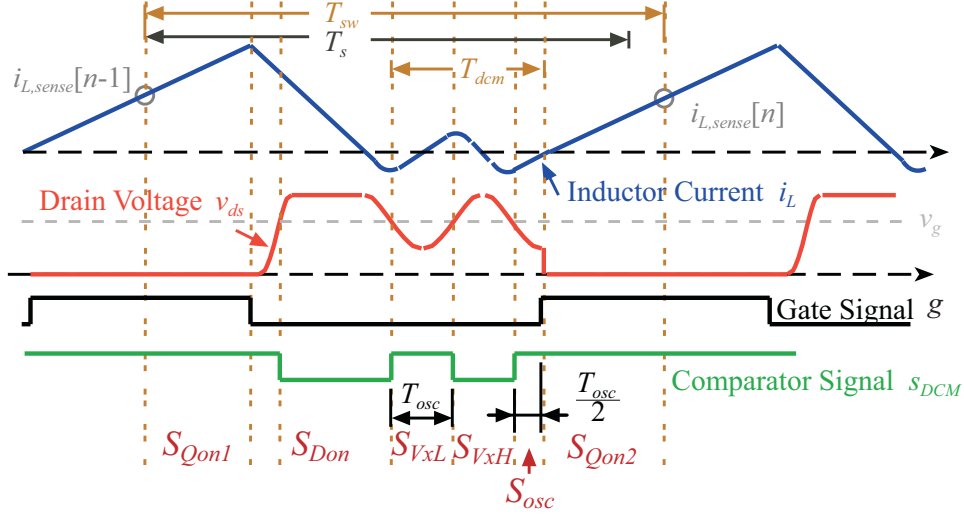


Figure 3.10: Operation waveforms of adaptive switching CCM/DCM current controller.

$$T_{on,ff} = \min \left[T_s \cdot \left(1 - \frac{v_g}{V_o} \right), T_s \cdot \sqrt{\left(1 - \frac{v_g}{V_o} \right) \cdot \frac{2Lu}{T_s}} \right]. \quad (3.20)$$

The approach described here is based on the assumption that the DCM oscillation period T_{osc} does not change much between two consecutive switching periods. The digital controller uses the DCM comparator signal s_{DCM} to measure and store the oscillation period T_{osc} . After expiration of the nominal (CCM) switching period T_s , the controller waits for a low-to-high transition of s_{DCM} , and extends the transistor turn-off time by $T_{osc}/2$ so that the next DCM oscillation cycle ends at the point when the inductor current is zero and the drain voltage is at a minimum, as shown in Fig. 3.10. The adaptive switching controller is implemented as a state machine, as shown in Fig. 3.11. Referring to the waveforms in Fig. 3.10, a switching period starts from the first transistor conduction state S_{Qon1} ; after the transistor is turned-off, the system is in the diode conduction state S_{Don} . If comparator signal s_{DCM} stays low for the entire transistor turn-off interval T_{off} , the system operates in CCM, ending the period in the second transistor conduction state S_{Qon2} . On the other hand, if DCM comparator output s_{DCM} flips to logic high before the end of T_{off} , the system operates in DCM. Depending on s_{DCM} , the state machine toggles between S_{VxL} and S_{VxH} to measure T_{osc} . Before moving to transistor turn-on state S_{Qon2} , the system waits for one half of T_{osc} to achieve valley switching at the minimum of v_{ds} ringing.

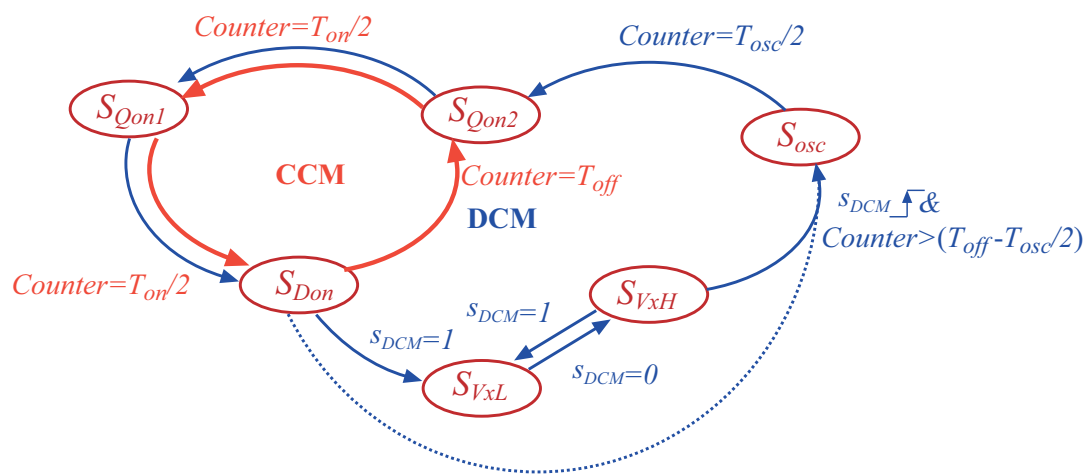


Figure 3.11: DPWM state machine of adaptive switching CCM/DCM current controller.

3.4 Current Loop Dynamics Improvement in DCM

Continuous-time averaged small-signal models for duty-cycle control to inductor current dynamics have been derived in [8, 48]. According to these models, compared to CCM dynamic response, the DCM response has a lower gain and does not include an integral term. Based on the discrete-time modeling approach in [52, 53], discrete-time small-signal responses including A/D sampling and modulator delay effects can be derived for CCM ($G_{idz-CCM}$) and DCM ($G_{idz-DCM}$) operation, as

$$G_{idz-CCM} = \frac{\hat{i}_L}{\hat{d}} = \frac{V_o T_s}{L} \cdot \frac{1}{z-1}, \quad (3.21)$$

$$G_{idz-DCM} = \frac{\hat{i}_L}{\hat{d}} = \frac{v_g T_s}{2L} \cdot \frac{1}{z}. \quad (3.22)$$

Using the fixed PI compensator G_{icz} , the corresponding current loop gain magnitude and phase responses for CCM and DCM operations are shown in Fig. 3.12. It can be observed that the gain and the cross-over frequency are much lower in DCM, resulting in poor current regulation and increased current distortion in DCM. This issue has been addressed in [48] by applying different compensators for DCM and for CCM operation, based on a CCM/DCM mode transition estimation. The estimation, however, may be subject to errors due to inductance tolerances or current sensing errors.

In order to maintain high current loop bandwidth in CCM and in DCM, a modified PI compensator (G_{icz-M}) is applied. The compensator parameters, α and β in Eq. 3.18, are adjusted based on the measured discontinuous conduction period T_{dcm} , thus eliminating possible mode estimation errors, as

$$\alpha_{dcm} = \frac{V_o - v_g}{v_g + V_{clamp}} \cdot \frac{T_s}{T_{on,ff}} \cdot \alpha, \quad (3.23)$$

$$\beta_{dcm} = -0.25. \quad (3.24)$$

In DCM, the compensator gain α_{dcm} is increased and the zero location β_{dcm} is shifted. V_{clamp} clamps the gain to a finite value around zero-crossings of the line voltage. Fig. 3.13 shows how the modification results in much improved bandwidth of the current control loop in DCM.

3.5 Results and Discussion

A 300W boost PFC rectifier ($f_s \approx 80$ kHz; $L = 0.5$ mH; $C = 220$ μ H) is built as shown in Fig. 3.14, using field programmable gate array (FPGA) development platform to implement the digital controller. Its experiment setup is shown in Fig. 3.15.

At heavy loads, in CCM operation, all of the controllers operate exactly the same as the constant frequency predictive current controller. They all result in low current harmonic distortion, as illustrated by Fig. 3.16 and Fig. 3.17.

At medium load to light load conditions, when DCM occurs for most of the ac line period, constant frequency operated predictive current controller with and without CCM/DCM current sensing correction are shown in Fig. 3.18(a) and Fig. 3.18(b), respectively. Current controller with CCM/DCM correction achieves lower current distortion. The DCM current sensing correction improves current control and reduces distortion.

Besides, in DCM, in contrast to the constant frequency operation (Fig. 3.19(a)) adaptive switching CCM/DCM current controller starts to turn the boost transistor at low switching node voltage in DCM, as illustrated by the experimental waveforms in Fig. 3.19(b).

At light loads, input current distortion using the adaptive switching CCM/DCM controller (Fig. 3.20(a)) is significantly reduced compared to the predictive CCM/DCM current controller (Fig. 3.20(b)). The DCM distortion is reduced by switching at the lowest drain voltage, thus reducing nonlinear effects of inductor current ringing on current regulation performance.

At very light load (5% rated power), DCM current distortion becomes more severe in constant

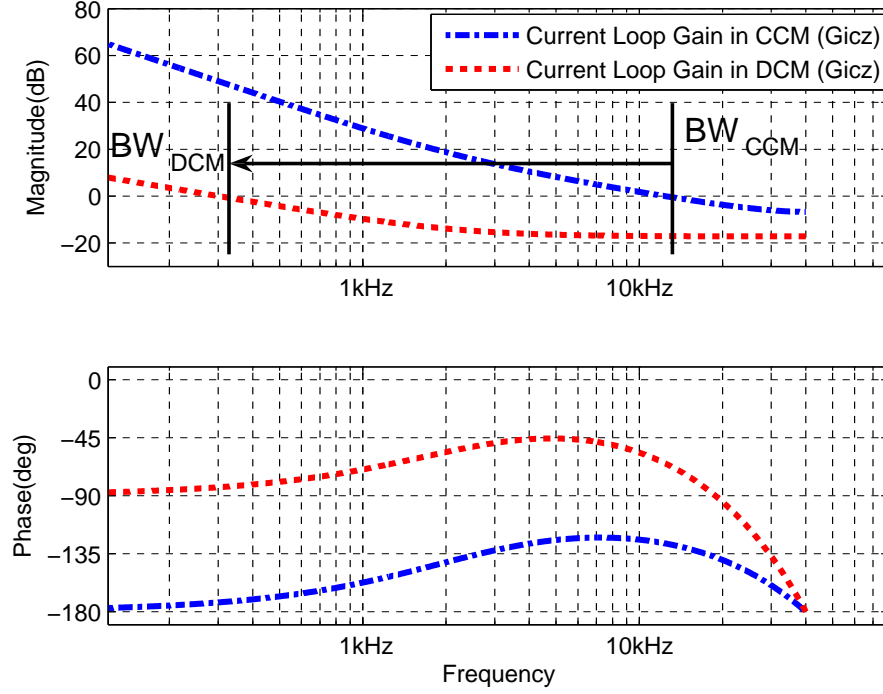


Figure 3.12: Current loop dynamics with current loop compensator G_{icz} in CCM (200 W) and DCM (80 W) ($f_s = 80$ kHz; $L = 0.5$ mH; $v_g = 100$ V).

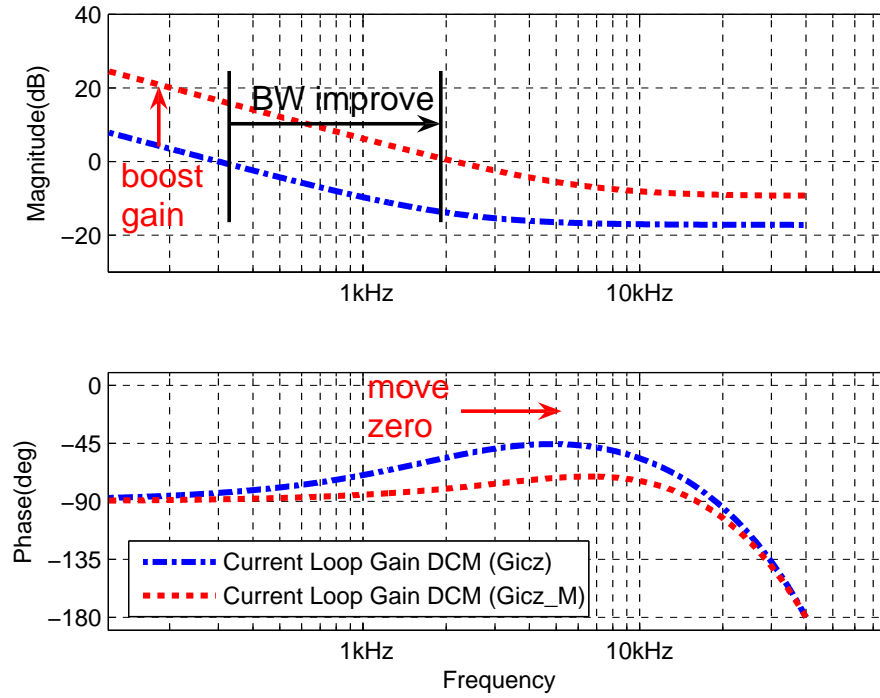


Figure 3.13: Current loop dynamics with current loop compensator G_{icz} and modified compensator G_{icz_M} in DCM (80 W) ($f_s = 80$ kHz; $L = 0.5$ mH; $v_g = 100$ V).

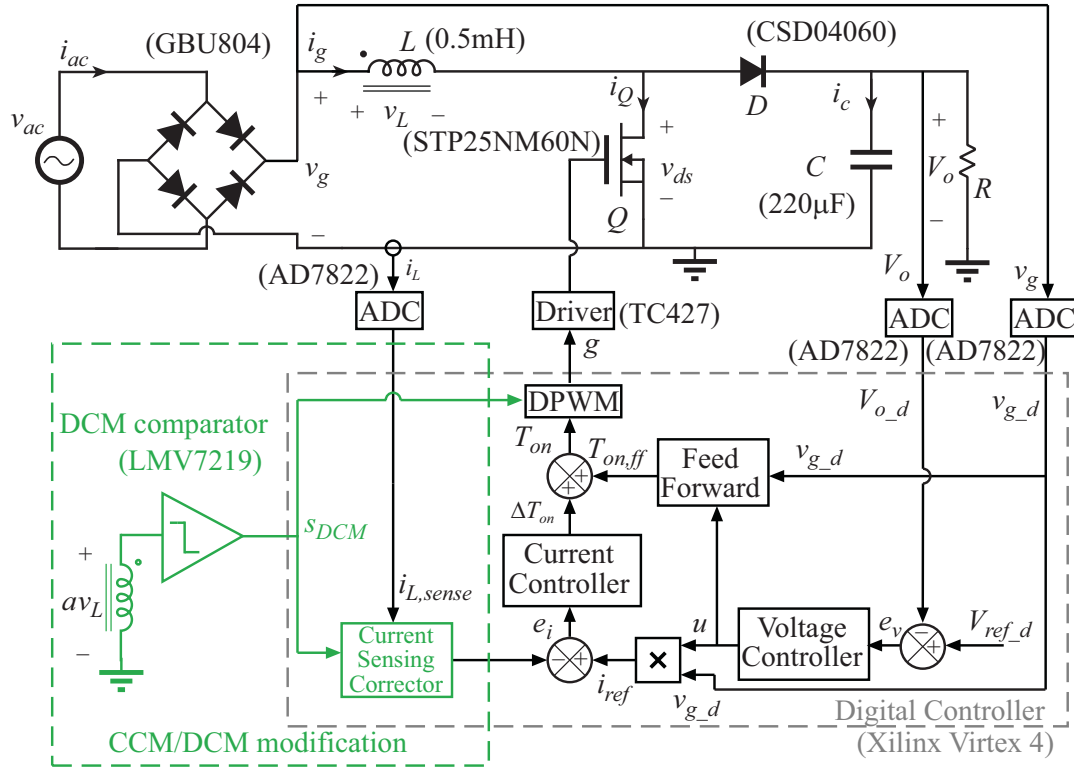


Figure 3.14: System block diagram on hardware implementation for adaptive switching current controller.

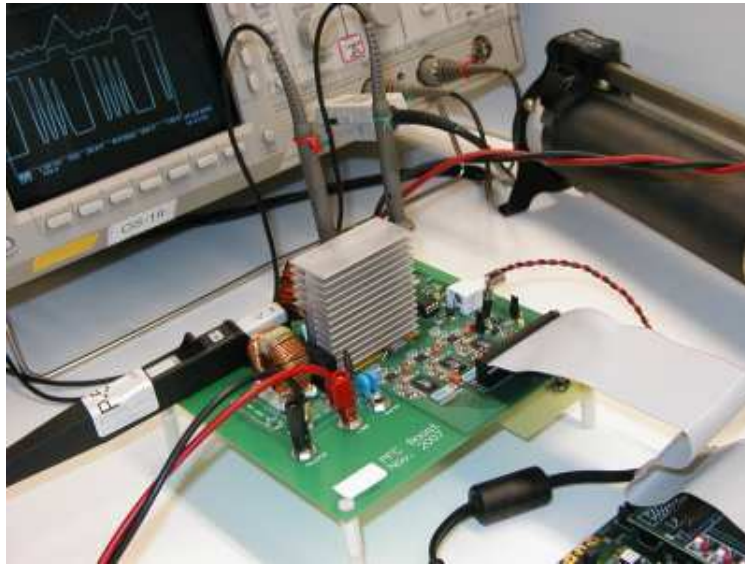


Figure 3.15: Evaluation board and experimental setup.

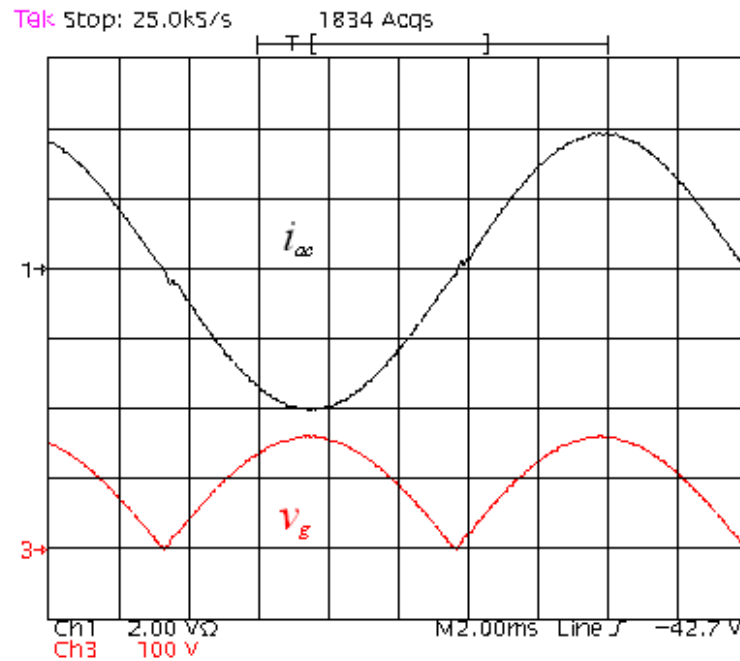


Figure 3.16: Experimental boost PFC converter waveforms, rectified line voltage v_g and line current i_{ac} , adaptive switching CCM/DCM controller ($f_s = 80$ kHz; 300 W).

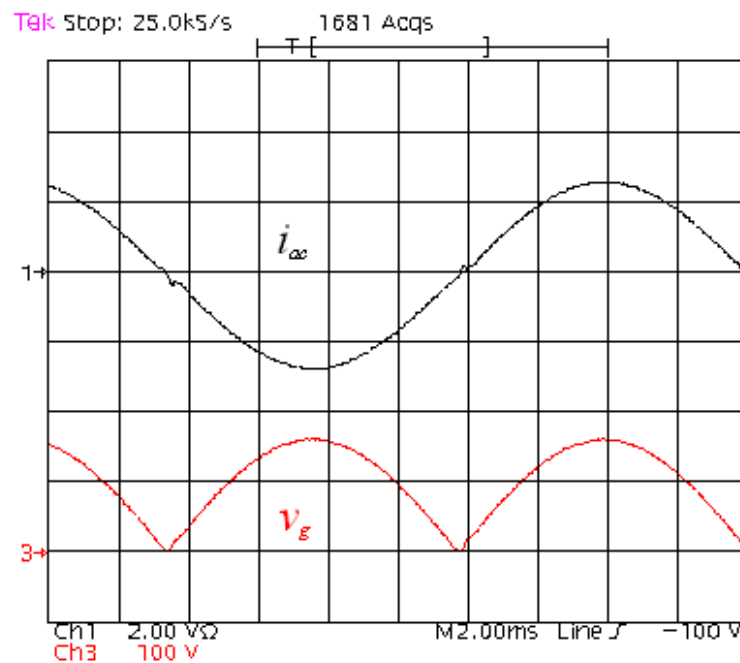
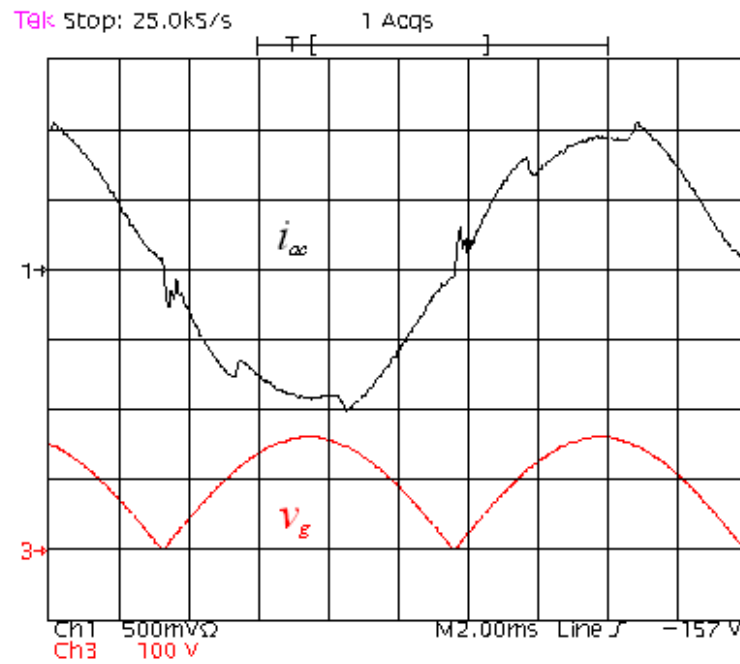
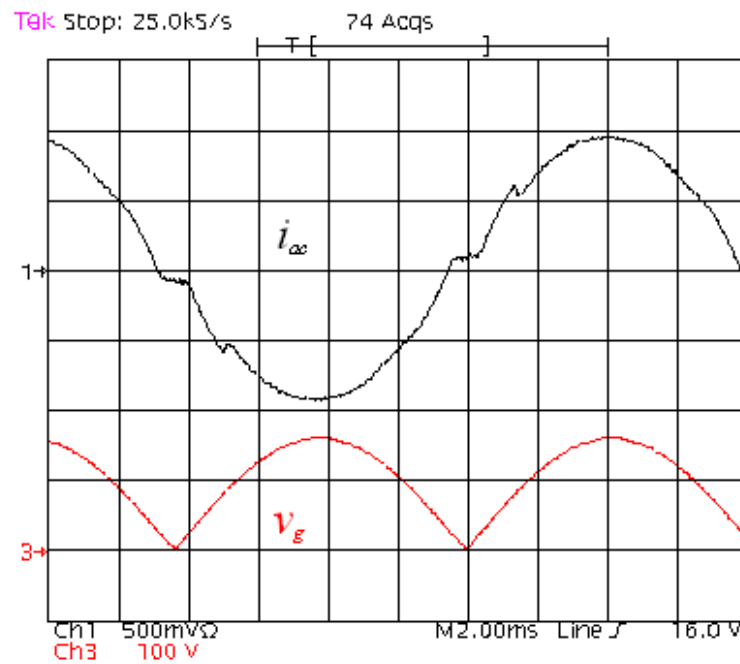


Figure 3.17: Experimental boost PFC converter waveforms, rectified line voltage v_g and line current i_{ac} , adaptive switching CCM/DCM controller ($f_s = 80$ kHz; 200 W).

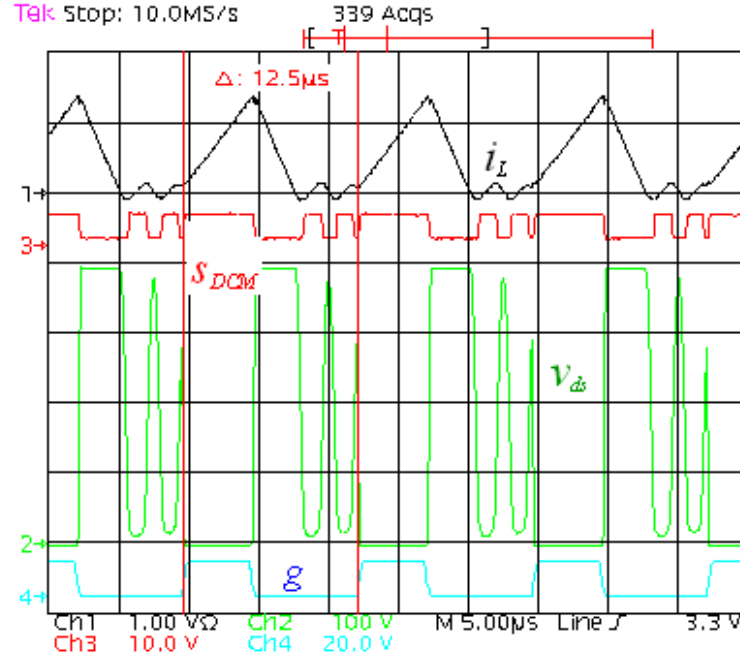


(a) Predictive current controller

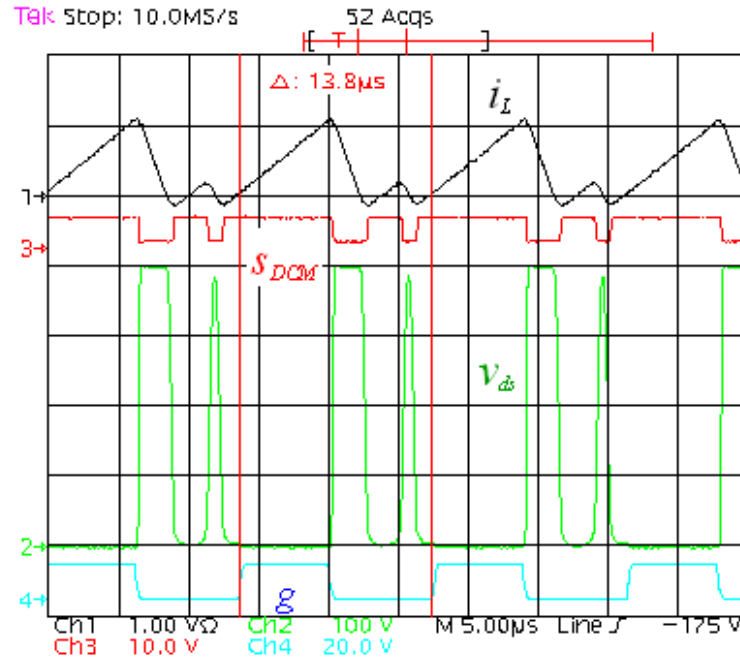


(b) Predictive CCM/DCM current controller

Figure 3.18: Experimental boost PFC converter waveforms, rectified line voltage v_g and line current i_{ac} ($f_s = 80$ kHz; 75 W).

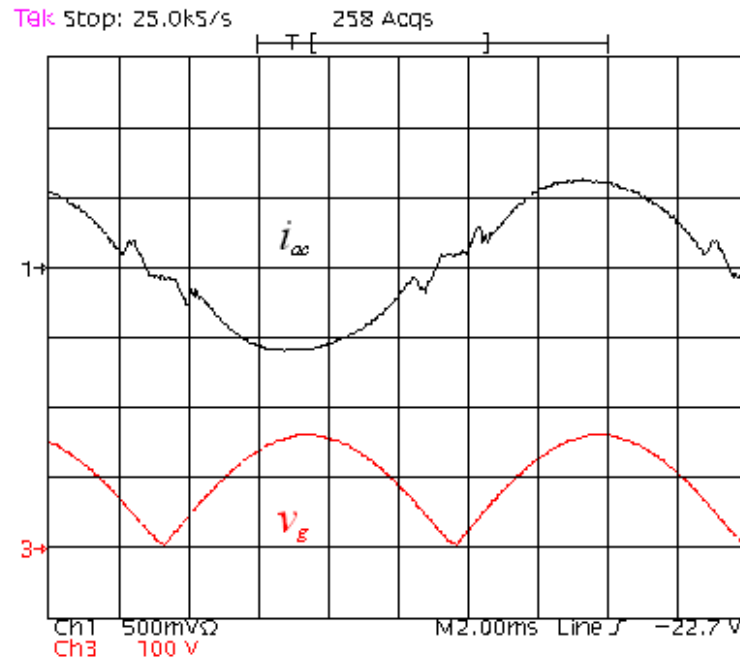


(a) Constant frequency predictive current controller

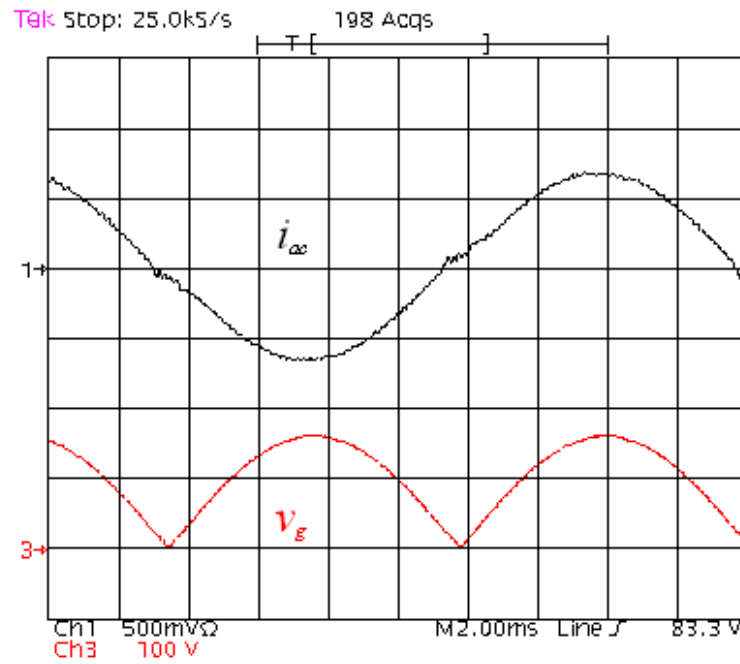


(b) Adaptive switching CCM/DCM current controller

Figure 3.19: Experimental boost PFC converter waveforms in DCM, inductor current i_L , switching node voltage v_{ds} , gate drive signal g and DCM comparator signal s_{DCM} ($f_s \approx 80$ kHz).



(a) Predictive CCM/DCM current controller



(b) Adaptive switching CCM/DCM current controller

Figure 3.20: Experimental boost PFC converter waveforms, rectified line voltage v_g and line current i_{ac} ($f_s = 80$ kHz; 50 W).

frequency operation, such as predictive current control (Fig. 3.21) and predictive CCM/DCM current control (Fig. 3.22). Adaptive switching reduces total current harmonic distortion dramatically, as shown in Fig. 3.23.

Fig. 3.24 compares the total harmonic distortion (THD) performance of the considered controllers, including predictive current control, predictive CCM/DCM current control, and adaptive switching CCM/DCM current control.

Some distortion over the line at light load case is a result of the discrete number of the oscillation periods allowed. With low current loop bandwidth in DCM, some distortion may occur as shown in Fig. 3.25(a). However, applying the modified current controller in DCM (Sec. 3.4) achieves an alternative number of oscillation periods and reduces the current harmonic distortion, as shown in Fig. 3.25(b).

For efficiency testing, the power stage has been tested with two different diode types, a fast soft recovery diode (FFPF04S60S) and a Silicon Carbide diode (CSD04060). The nominal switching frequency in the experimental setup is 80 kHz. Measured efficiency as a function of output power is compared in Fig. 3.26 for the considered control approaches. As expected, at high loads, efficiency is slightly better with the Silicon Carbide diode because reverse recovery losses are lower. At intermediate and light loads, when the converter operates in DCM most of the time, losses due to the switch-node capacitance are more significant. As a result, the adaptive switching approach offers more significant efficiency improvements with the Silicon Carbide diode, which has a larger capacitance. Results are summarized in Table 3.1.

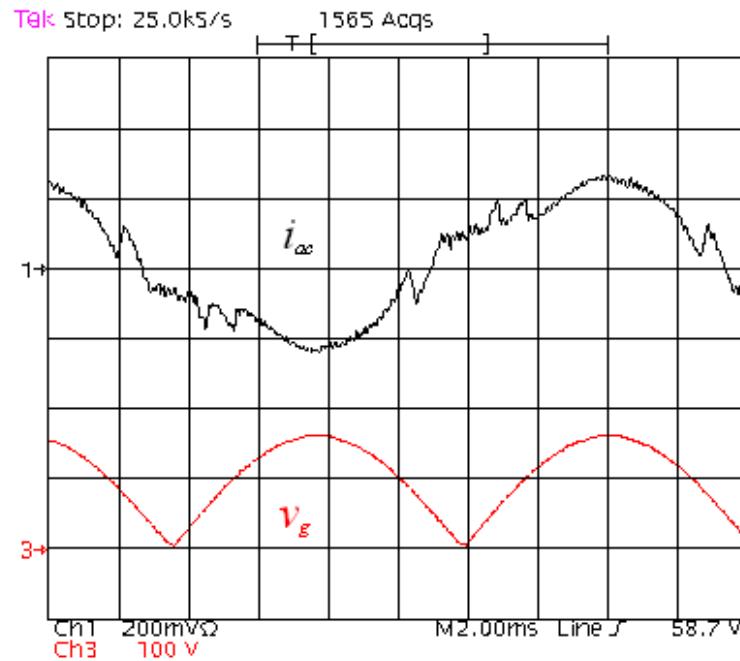


Figure 3.21: Experimental boost PFC converter waveforms, rectified line voltage v_g and line current i_{ac} , predictive current controller ($f_s = 80$ kHz; 15 W).

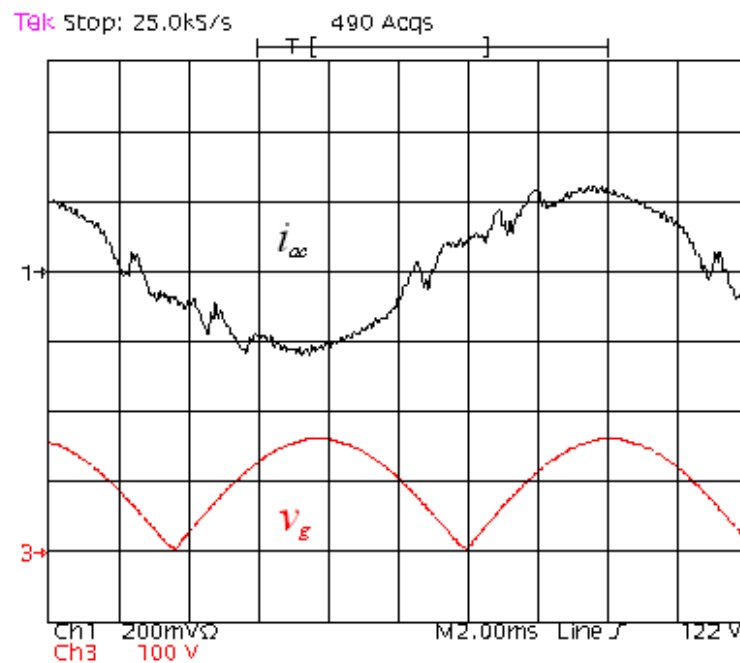


Figure 3.22: Experimental boost PFC converter waveforms, rectified line voltage v_g and line current i_{ac} , predictive CCM/DCM current controller ($f_s = 80$ kHz; 15 W).

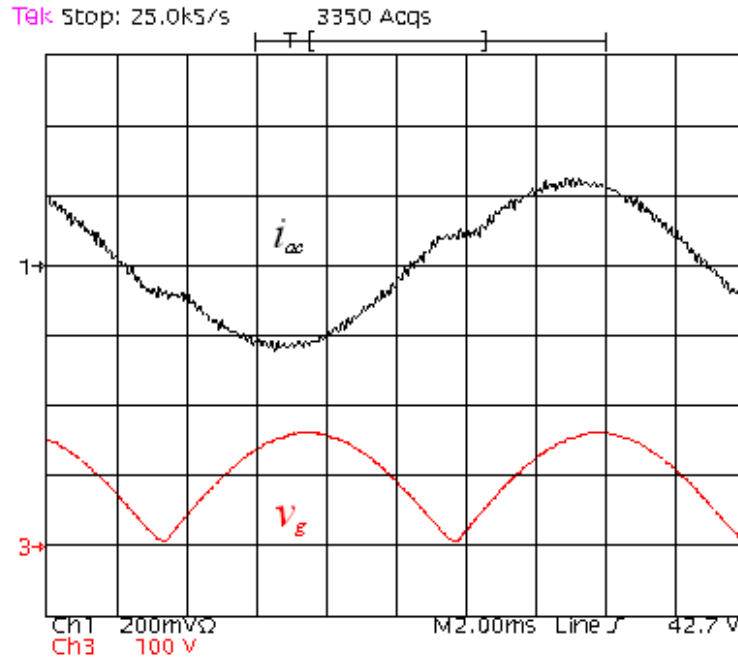


Figure 3.23: Experimental boost PFC converter waveforms, rectified line voltage v_g and line current i_{ac} , adaptive switching CCM/DCM controller ($f_s = 80$ kHz; 15 W).

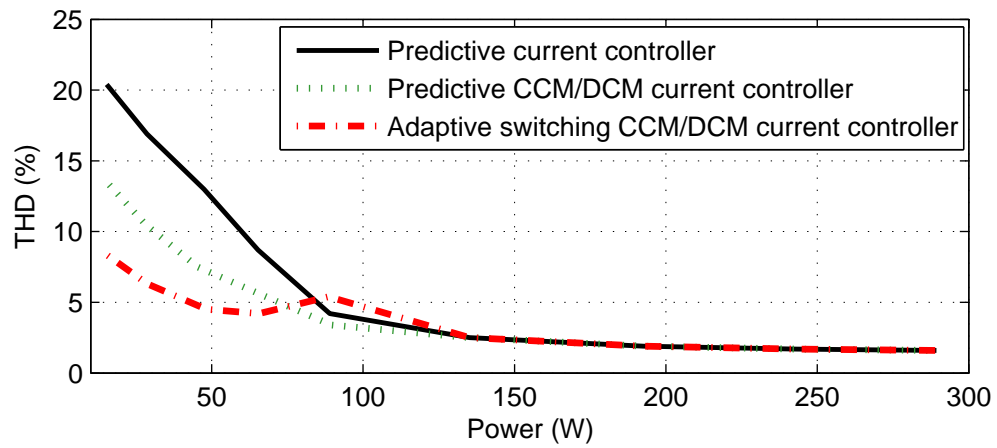
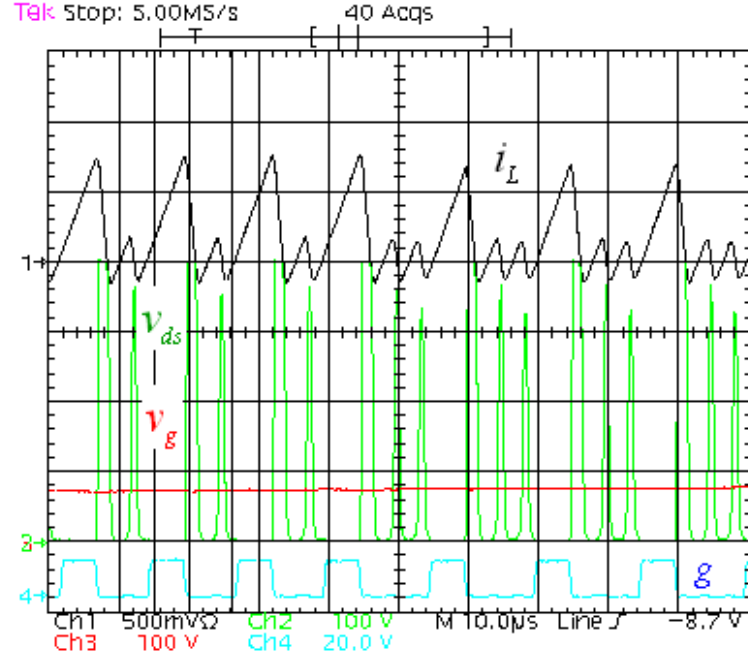
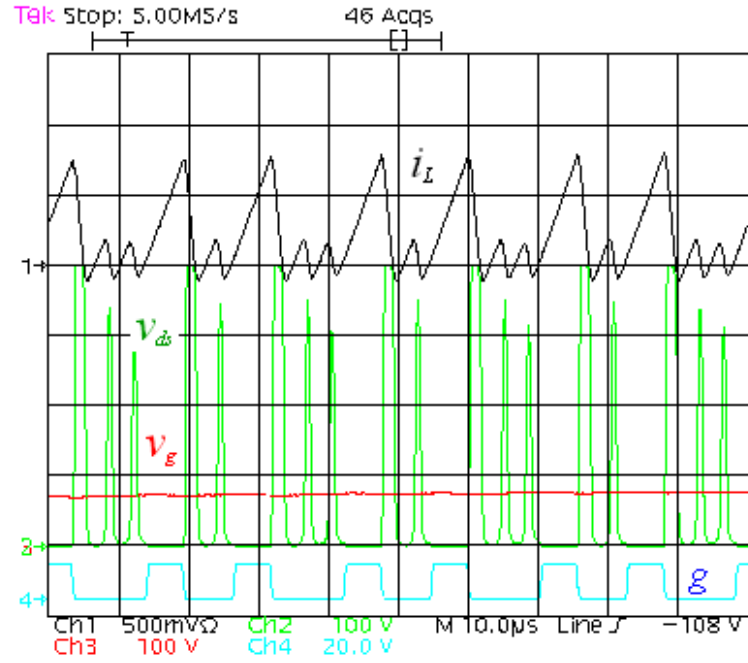


Figure 3.24: Current harmonic distortion comparison ($v_{g-rms} = 115$ V; $f_s = 80$ kHz).



(a) Adaptive switching CCM/DCM current controller with regular controller G_{icz}



(b) Adaptive switching CCM/DCM current controller with modified controller G_{icz-M}

Figure 3.25: Experimental boost PFC converter waveforms in DCM, inductor current i_L , switching node voltage v_{ds} , gate drive signal g and rectified input voltage v_g ($f_s \approx 80$ kHz).

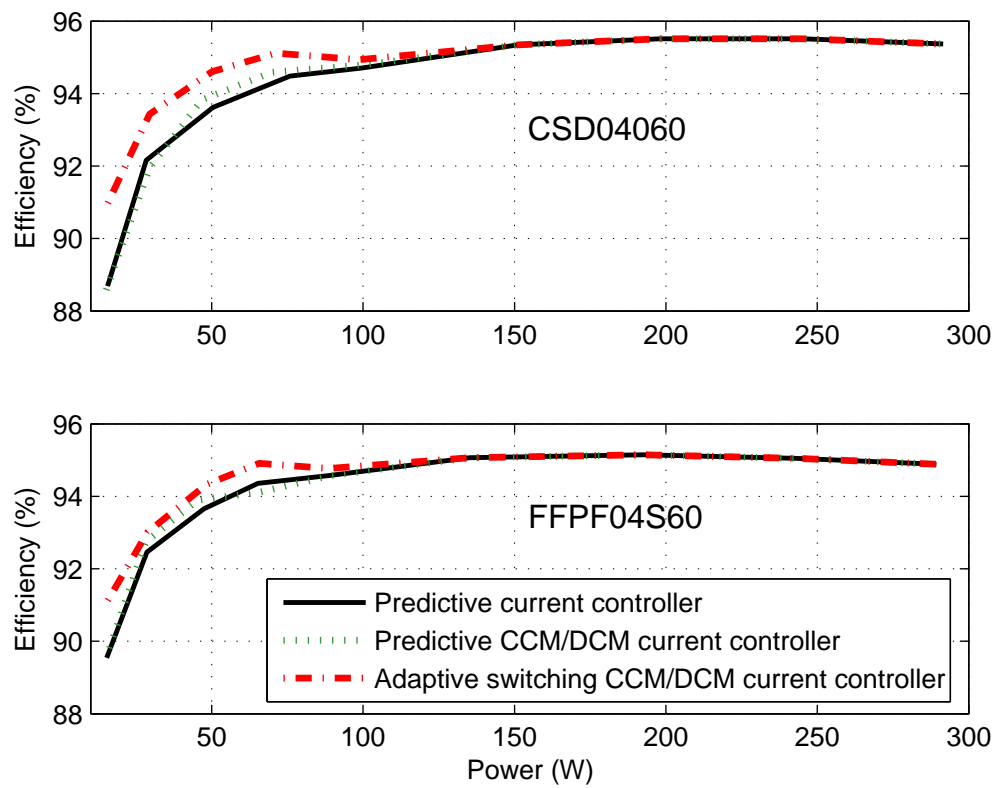


Figure 3.26: Efficiency comparison ($v_{g-rms} = 115$ V; $f_s = 80$ kHz).

	Power	Efficiency	Power Factor	THD
CCM Predictive Current Control	300W	95.3%	0.999	2.2%
CCM/DCM Predictive Current Control	300W	95.3%	0.999	2.2%
Adaptive Switching CCM/DCM Current Control	300W	95.3%	0.999	2.2%
CCM Predictive Current Control	150W	94.7%	0.999	2.8%
CCM/DCM Predictive Current Control	150W	94.5%	0.999	2.8%
Adaptive Switching CCM/DCM Current Control	150W	95.1%	0.999	2.8%
CCM Predictive Current Control	50W	93.6%	0.987	15.9%
CCM/DCM Predictive Current Control	50W	93.8%	0.994	7.3%
Adaptive Switching CCM/DCM Current Control	50W	94.6%	0.994	5.9%
CCM Predictive Current Control	15W	88.6%	0.950	21.2%
CCM/DCM Predictive Current Control	15W	88.6%	0.933	15.6%
Adaptive Switching CCM/DCM Current Control	15W	91.0%	0.937	10.7%

Table 3.1: Performance comparison of experimental CCM predictive current controller, CCM/DCM predictive current controller and adaptive switching CCM/DCM current controller ($v_{ac,rms} = 115V$; $f_s = 80kHz$)(transistor: STP25NM60N; diode: CSD04060).

Chapter 4

Adaptive Frequency CCM/DCM Current Control in Boost PFC

At light load, switching loss is usually the dominant part of the power loss. Pulse frequency modulation (PFM) reduces the switching frequency to reduce the switching loss at light load. PFM is a well-known control approach to improve light load efficiency in DC-DC converters [54–56]. Similar ideas have been applied in power factor correction (PFC) rectifiers. One approach is the burst mode, which reduces the equivalent switching frequency [41]. Another approach is the conduction angle control, which keeps the transistor turned-off around input voltage zero-crossings to improve efficiency [42]. In the constant on-time control, the switching frequency is adjusted based on the load [31, 57].

Burst mode and conduction angle control results in higher current distortion; the constant on-time approach reduces the switching frequency only based on the load. However, within the line period (T_L), since the PFC rectifiers regulate the input current (i_g) to follow the waveshape of the input voltage (v_g), the power level processed around peak line voltage is quite different from that around line voltage zero crossing. In order to reduce the light load switching loss based on the overall power level and instantaneous transmitted power level, a new approach is introduced in this chapter. Sec. 4.1 addresses the principles of the adaptive frequency approach, which combines PFM and current shaping. Then, details of the adaptive frequency CCM/DCM current control are presented in Sec. 4.2. Experimental results are given in Sec. 4.3.

4.1 PFM and Current shaping

In regular pulse width modulation (PWM) converters, constant frequency operation makes the converter efficiency drop dramatically at light load. The conduction loss reduces with the power level; however, since the switching loss is a strong function of operating frequency, the switching loss does not change much with different power levels. Once the switching loss dominates the system loss, the overall efficiency decreases dramatically. As a result, converters operating at high switching frequency tend to have lower efficiency at light load. On the other hand, low frequency operated converters have high current stress and introduce more conduction loss at heavy load.

To achieve high efficiency for wide load range, PWM plus PFM approaches have been developed in DC-DC switched-mode converters [54–56]. The PWM plus PFM approach combines constant frequency PWM operation at heavy load and PFM operation at light load.

Adaptive frequency approach is similar to the PWM plus PFM approach. At heavy load, when the boost converter is operated in continuous conduction mode (CCM), it runs the regular predictive current control (PCC); while at light load, when the boost converter is operated in discontinuous conduction mode (DCM), it adjusts the operating frequency.

The main idea of the adaptive frequency approach is based on using switching frequency to shape the inductor current instead of using duty ratio (Fig. 4.1). Generally, constant frequency PFC controller directly shapes the inductor current by the duty ratio (d_{DCM}) in DCM, as

$$d_{DCM} = \sqrt{\frac{2L}{R_e T_s} \cdot \left(1 - \frac{v_g}{V_o}\right)}, \quad (4.1)$$

which requires the power command ($u=1/R_e$) and rectified input voltage (v_g) information.

Instead of using the duty ratio to shape the inductor current, the proposed adaptive frequency approach extends the minimum switching period (T_s), to shape the inductor current. By applying the same transistor conduction period (T_{on}) as in the regular CCM operation and by changing the switching period in DCM ($T_{s,DCM}$), the adaptive frequency approach makes the average current ($\langle i_L \rangle_{T_s}$) the same as in constant frequency case, as illustrated in Fig. 4.1.

To achieve correct current shaping, the required turn-on period has to be

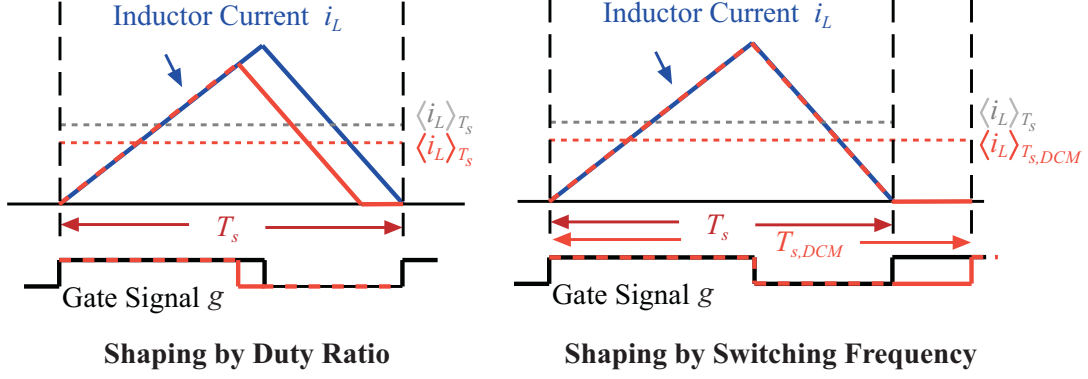


Figure 4.1: DCM current shaping by duty ratio or shaping by switching frequency.

$$T_{on,DCM} = T_s \cdot \left(1 - \frac{v_g}{V_o}\right) = d_{DCM} \cdot T_{s,DCM}. \quad (4.2)$$

Therefore, the DCM switching frequency of the adaptive frequency approach ($T_{s,DCM}$) has to be adjusted as

$$T_{s,DCM} = T_s^2 \cdot \left(1 - \frac{v_g}{V_o}\right) \cdot \frac{R_e}{2L}. \quad (4.3)$$

In the proposed adaptive frequency approach, the CCM switching frequency is constant, $f_{smax} = 1/T_{s,min}$. The DCM switching frequency variation is based on keeping the transistor duty cycle constant. Fig. 4.2 shows variations of the transistor duty ratio and the switching period over one half of the line period at an intermediate load. When the converter operates at heavy load under constant frequency operation in CCM, the switch duty ratio is approximately independent of load. In DCM, with constant frequency operation, a lower duty ratio is required as the load is reduced. The proposed adaptive frequency controller keeps the same duty ratio during DCM operation,

$$D_{DCM} = \frac{T_{on}}{T_{s,DCM}} = \frac{2L}{R_e T_s}, \quad (4.4)$$

but allows the switching period to vary as Eq. 4.3. Note that the constant DCM duty ratio approach also enables a smooth transition between constant-frequency CCM and variable-frequency DCM

operation of the controller. The switching frequency variation is shown in the bottom part of Fig. 4.2, while the corresponding duty ratio variation is shown in the top part of Fig. 4.2.

A light load example is shown in Fig. 4.3. As opposed to constant frequency operation, where current shaping is accomplished by adjusting the duty ratio, the switching period is adjusted in the adaptive frequency technique.

At very light loads, depending on the selection of the maximum switching frequency $f_{s,max}$ and inductance value L , the adaptive frequency CCM/DCM controller may operate below 20 kHz, which may result in audible noise. A limit to the maximum allowed switching period ($T_{s,max}$) is imposed to limit the minimum allowed switching frequency, as shown in Fig. 4.4. When the adaptive frequency controller hits the lower frequency limit at very light loads, current shaping is based on the current feedback only, without the feed-forward term.

4.2 Adaptive Frequency CCM / DCM Current Control

The adaptive frequency CCM/DCM controller is also taking advantage of the adaptive switching CCM/DCM control described in Chapter 3. The adaptive frequency CCM/DCM controller applies the current sensing error correction and makes boost transistor turn on at the lowest drain voltage. The system block diagram and current controller block diagram are shown in Fig. 4.5 and Fig. 4.6 respectively, which make use of the same hardware implementation as the adaptive switching approach.

Adding the lower frequency limitation, the complete set of adaptive frequency CCM/DCM controller equations is as follows:

$$T_{on}[n+1] = \Delta T_{on}[n] + T_{on,ff}, \quad (4.5)$$

$$T_s[n+1] = \mathbf{max}[T_{s,min}, T_{s,DCM}], \quad (4.6)$$

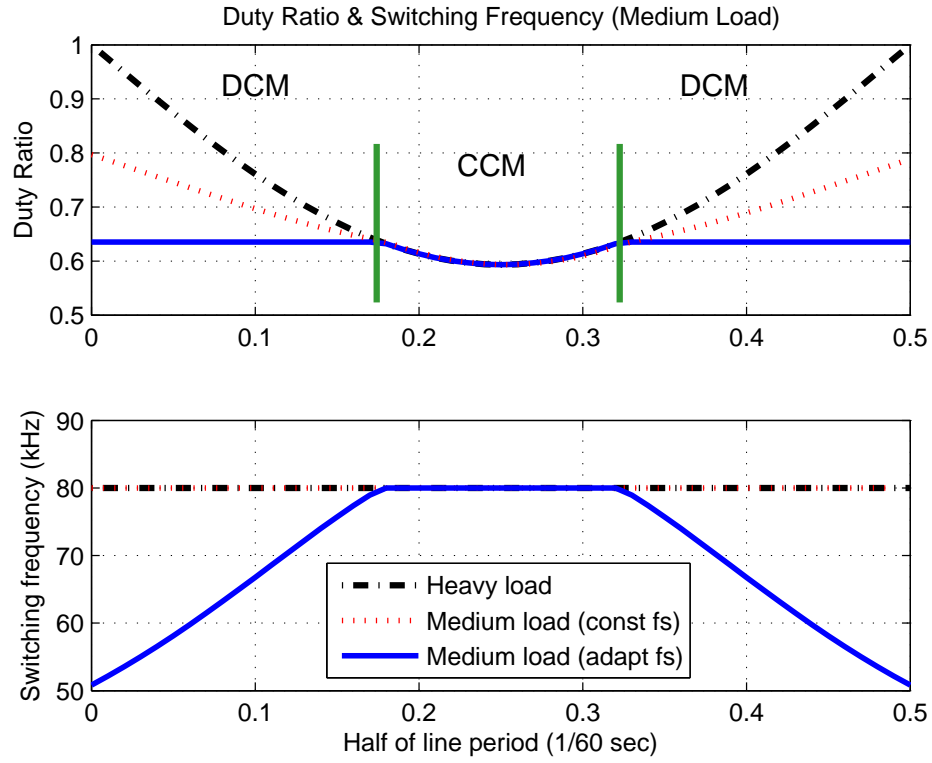


Figure 4.2: Duty ratio and switching frequency variations over half of the line period; comparison of constant frequency and adaptive frequency operation at medium load ($v_{g-rms} = 115$ V; $f_{s,max} = 80$ kHz; 105 W).

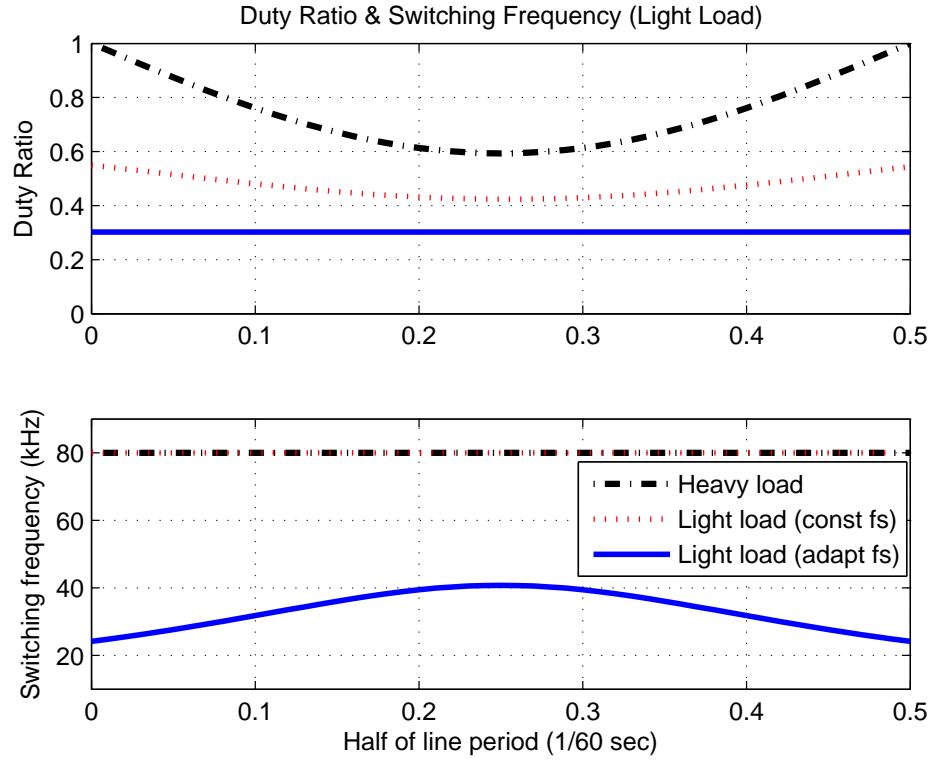


Figure 4.3: Duty ratio and switching frequency variations over half of the line period; comparison of constant frequency and adaptive frequency operation at light load ($v_{g-rms} = 115$ V; $f_{s,max} = 80$ kHz; 50 W).

$$T_{s,DCM} = \min \left[T_{s,max}, T_{s,min}^2 \left(1 - \frac{v_g}{V_o} \right) \frac{R_e}{2L} \right], \quad (4.7)$$

$$T_{on}[n] = \alpha \cdot e_i[n] + \alpha \cdot \beta \cdot e_i[n-1] + \Delta T_{on}[n-1], \quad (4.8)$$

$$e_i[n] = T_{sw}[n] \cdot i_{ref} - (T_{sw}[n] - T_{dcm}[n]) \cdot i_{L,sense}, \quad (4.9)$$

$$T_{on,ff} = \min \left[\left(1 - \frac{v_g}{V_o} \right) \cdot T_{s,min}, 2L \cdot u \cdot \frac{T_{s,max}}{T_{s,min}} \right], \quad (4.10)$$

where $T_{s,min}$ is the constant switching period selected for CCM operation, $T_{s,max}$ is the maximum allowed switching period. In DCM, coefficients α and β are adjusted according to DCM current controller shown in Chapter 3. Notice that adaptive frequency does not require complex digital operations, such as square root calculation and fast divider operation. The only divider operation required is R_e , which is one over power command (u), as Eq. 4.7. In the digital voltage loop, u updates once per line period. Therefore, using a multiplication and a feedback loop is a cost effective approach to implement divider operation .

4.3 Results and Discussion

A 300W boost PFC rectifier ($f_{s,max} \approx 80$ kHz; $f_{s,min} \approx 20$ kHz; $L = 0.5$ mH; $C = 220$ μ H) built for adaptive switching CCM/DCM current control (Chapter 3), also works as the platform to demonstrate adaptive frequency CCM/DCM current control. System block diagram with component information is shown in Fig. 4.7.

To demonstrate operation of the adaptive frequency approach, experimental waveforms, ac line current i_{ac} and rectified line voltage v_g , are shown in Fig. 4.8(a) and Fig. 4.8(b). Because the adaptive frequency CCM/DCM current control is also taking advantage of the adaptive switching

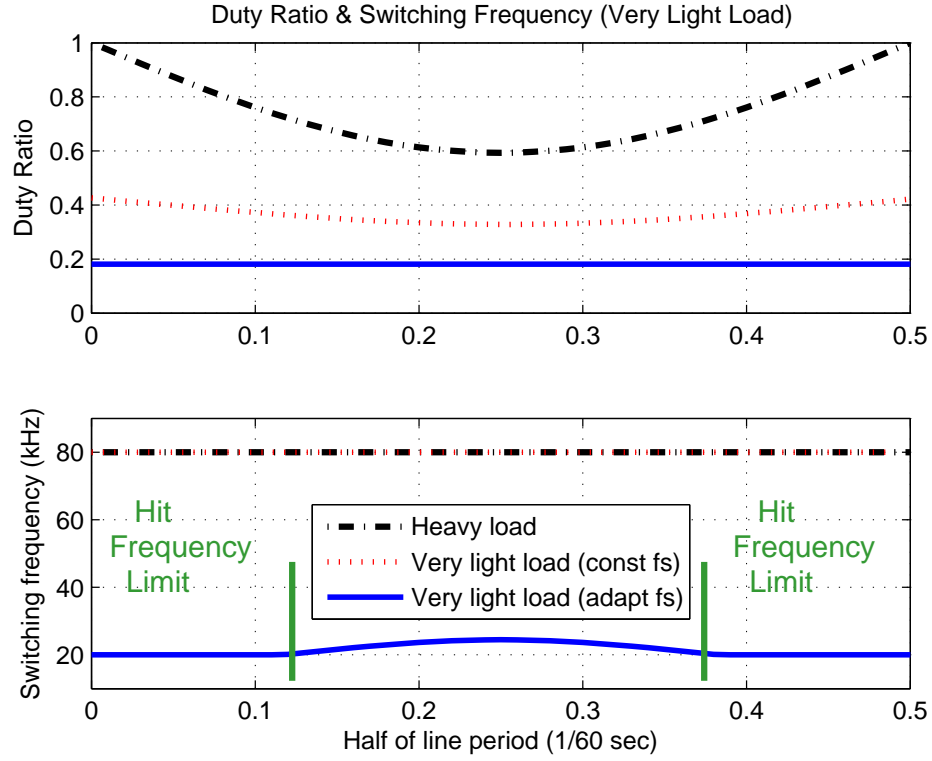


Figure 4.4: Duty ratio and switching frequency variations over half of the line period; comparison of constant frequency and adaptive frequency operation at very light load ($v_{g-rms} = 115$ V; $f_{s,max} = 80$ kHz; 30 W).

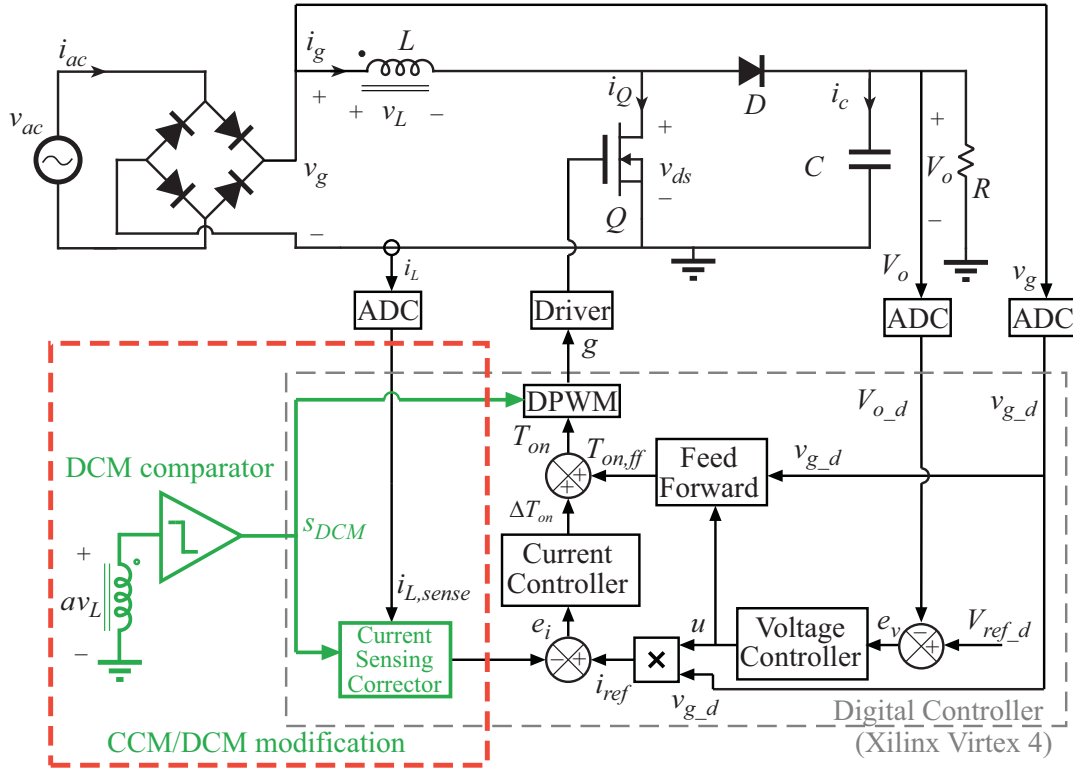


Figure 4.5: System block diagram for adaptive frequency current controller.

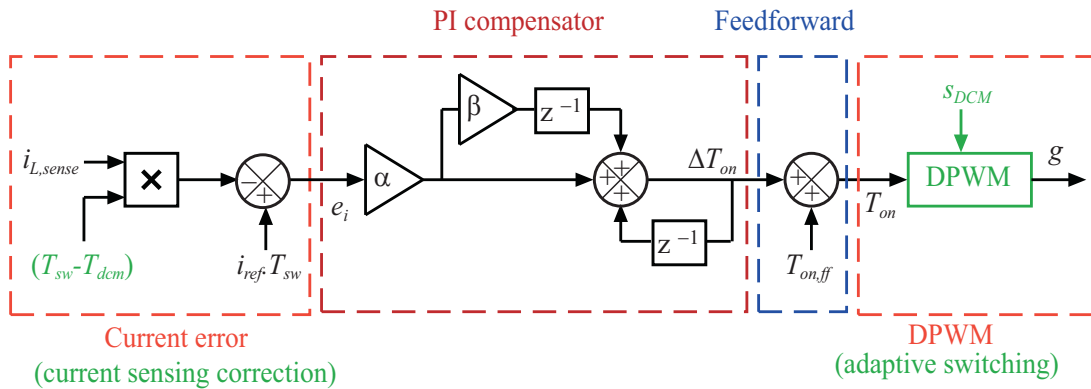


Figure 4.6: Block diagram of current controller (adaptive frequency CCM/DCM current control).

CCM/DCM control to form the low voltage switching, compared with constant frequency predictive current control (Fig. 4.8(a)), the adaptive frequency CCM/DCM current control reduces the current harmonic distortion dramatically (Fig. 4.8(b)).

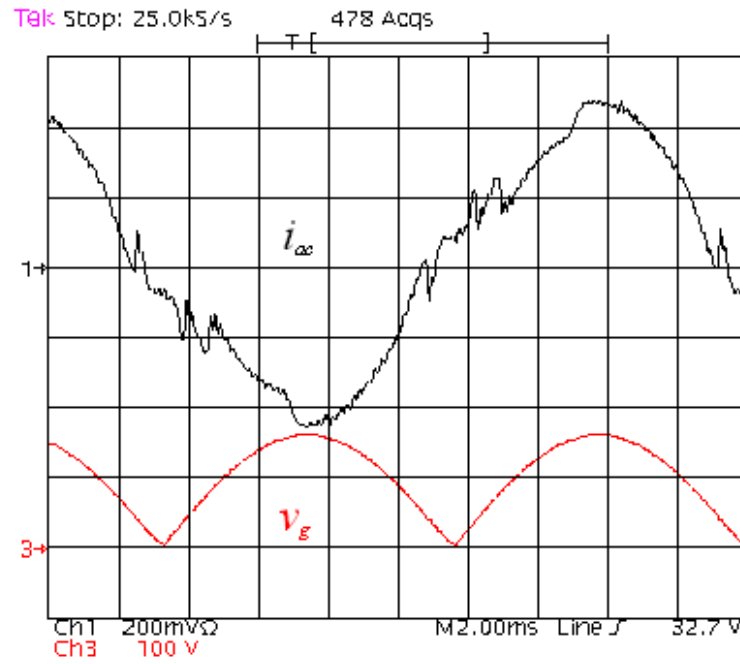
A zoom-in of the waveforms at the top of the line period shown in Fig. 4.8(b) shows the valley voltage switching with the switching frequency of about 54 kHz (Fig. 4.9(a)). A zoom in closer to the zero-crossing of the ac line voltage in Fig. 4.8(b) shows how the switching frequency is reduced to about 37 kHz (Fig. 4.9(b)).

Fig. 4.9(a) and Fig. 4.9(b) also show significant changes in the DCM oscillation period T_{osc} at different operating points, which is a result of the fact that the switch-node capacitance is highly nonlinear. Therefore, as discussed in Chapter 3, the proposed adaptive switching approach based on on-line measurement of the oscillation period has advantages over fixed delay approaches previously applied to AC-DC PFC rectifiers [32, 33, 51].

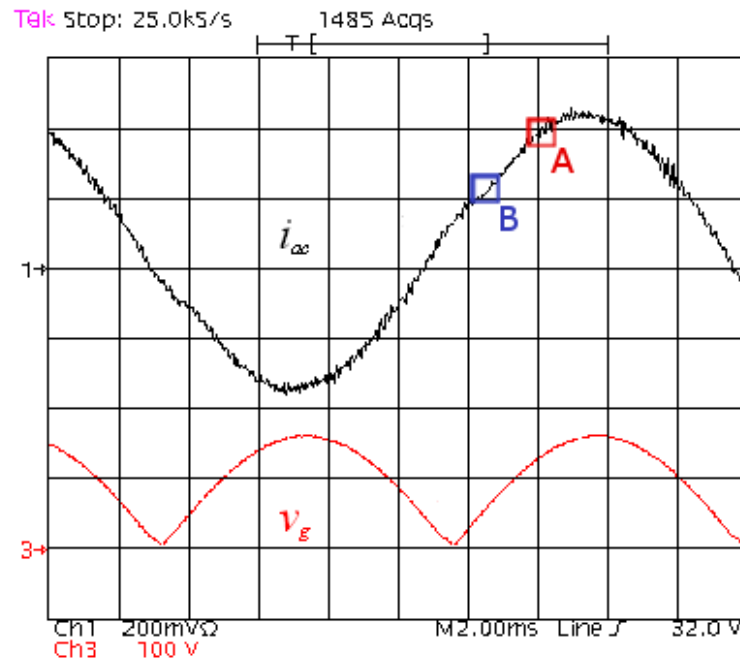
At very light load (5% rated power), adaptive frequency CCM/DCM current controller shapes the inductor current by the current feedback only. When operating frequency reaches its lowest boundary, the adaptive frequency CCM/DCM current controller keeps the same feed forward term. More current harmonic distortion is introduced compared to the adaptive switching CCM/DCM current control shown in Chapter 3 (Fig. 4.10).

Fig. 4.11 compares the total harmonic distortion (THD) performance of the considered controllers, including the predictive current control, the predictive CCM/DCM current control, the adaptive switching CCM/DCM current control, and the adaptive frequency CCM/DCM current control.

For efficiency testing, the same as the adaptive switching CCM/DCM current control shown in Chapter 3, two different diodes have been tested, including a fast soft recovery diode (FFPF04S60S) and a Silicon Carbide diode (CSD04060). The nominal switching frequency in the experimental setup is 80 kHz; the minimum switching frequency in the adaptive frequency controller is set to 20 kHz. Measured efficiency as a function of output power is compared in Fig. 4.12 for the considered control approaches. Adaptive frequency CCM/DCM current controller offers even more

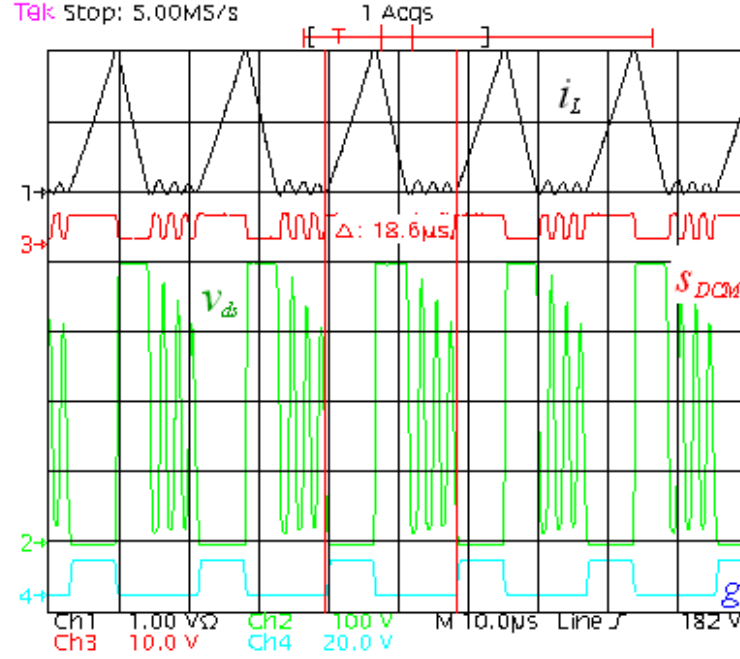


(a) Predictive current controller

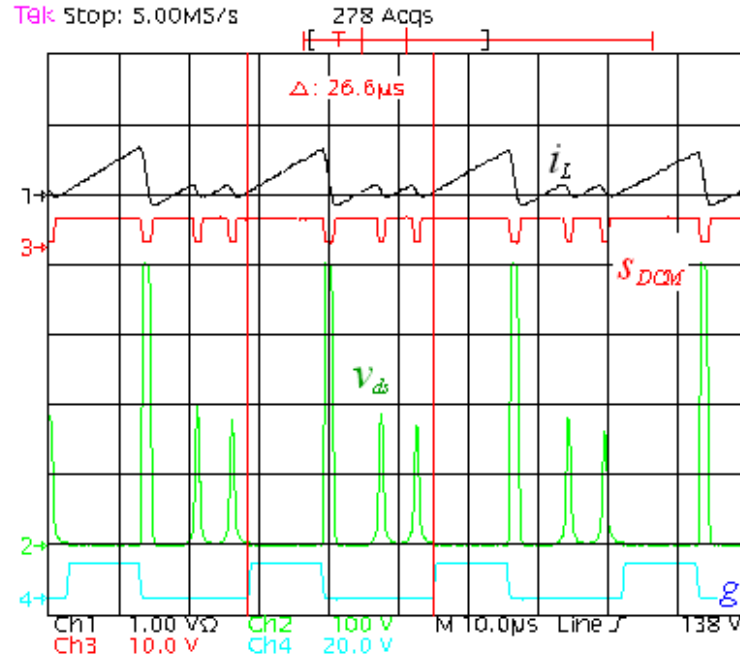


(b) Adaptive frequency CCM/DCM current controller

Figure 4.8: Experimental boost PFC converter waveforms, rectified line voltage v_g and line current i_{ac} ($f_{s,max} = 80$ kHz; $f_{s,min} = 20$ kHz; 30 W).



(a) Operation at 54 kHz at high input voltage, point A



(b) Operation at 37 kHz at low input voltage, point B

Figure 4.9: Experimental boost PFC converter waveforms in DCM using adaptive frequency CCM/DCM current controller, corresponding to Fig. 4.8(b), inductor current i_L , switching node voltage v_{ds} , gate drive signal g and DCM comparator signal s_{DCM} ($f_{s,max} = 80$ kHz; $f_{s,min} = 20$ kHz; 30 W).

efficiency improvements compared to the adaptive switching CCM/DCM current controller. The results are summarized in Table 4.1.

In comparison of the system complexity, Table 4.2 lists the total equivalent gate count of the controllers. The DCM feed-forward term, which requires a square root operation, increases the number of gate count in both CCM/DCM predictive current controller and adaptive switching CCM/DCM current controller in Chapter 3. Although adaptive frequency CCM/DCM current controller always uses the CCM feed-forward term, it requires some multiplication operations to calculate the switching period in DCM. Nevertheless, with some extra complexity (DCM comparator) and less than 1/3 extra area in digital circuitry (Table 4.2), it can achieve high efficiency and low harmonic distortion over wide range of loads.

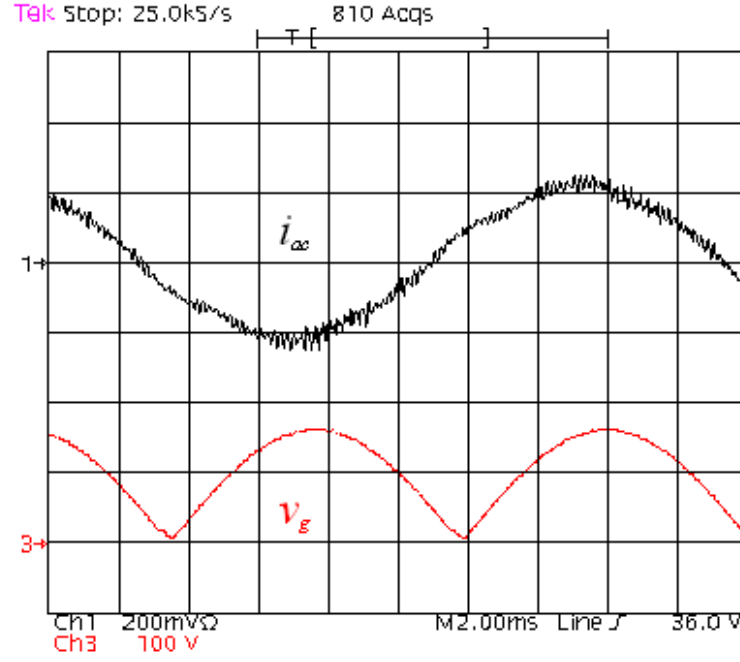


Figure 4.10: Experimental boost PFC converter waveforms, rectified line voltage v_g and line current i_{ac} , adaptive frequency CCM/DCM current controller ($f_{s,max} = 80$ kHz; $f_{s,min} = 20$ kHz; 15 W).

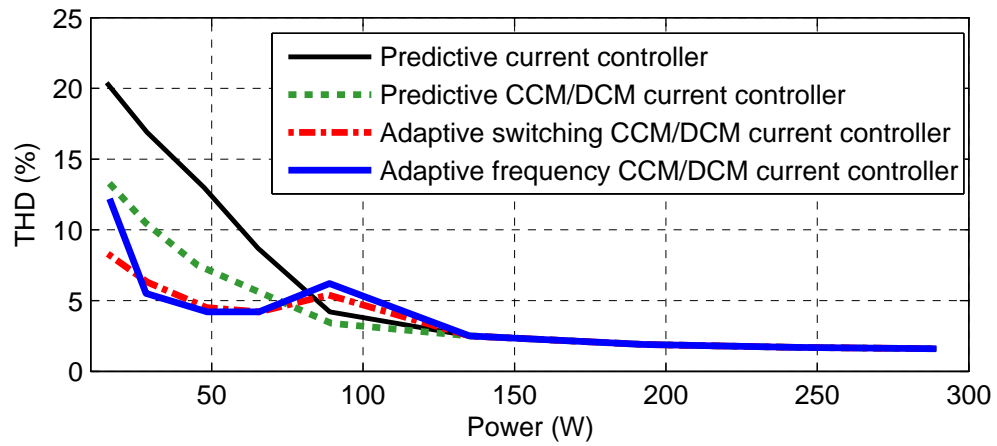


Figure 4.11: Current harmonic distortion comparison ($v_{g-rms} = 115$ V; $f_s = 80$ kHz).

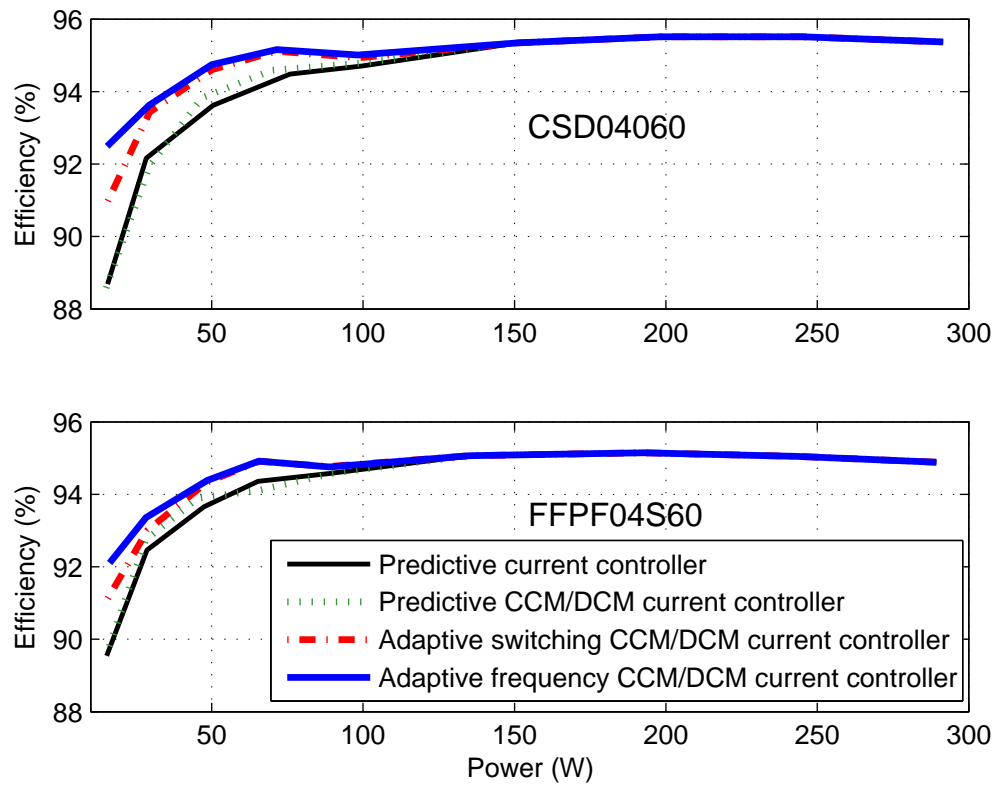


Figure 4.12: Efficiency comparison ($v_{g-rms}=115$ V; $f_{s,max} = 80$ kHz; $f_{s,min} = 20$ kHz).

	Power	Efficiency	Power Factor	THD
CCM Predictive Current Control	300W	95.3%	0.999	2.2%
CCM/DCM Predictive Current Control	300W	95.3%	0.999	2.2%
Adaptive Switching CCM/DCM Current Control	300W	95.3%	0.999	2.2%
Adaptive Frequency CCM/DCM Current Control	300W	95.3%	0.999	2.2%
CCM Predictive Current Control	150W	94.7%	0.999	2.8%
CCM/DCM Predictive Current Control	150W	94.5%	0.999	2.8%
Adaptive Switching CCM/DCM Current Control	150W	95.1%	0.999	2.8%
Adaptive Frequency CCM/DCM Current Control	150W	95.1%	0.999	2.8%
CCM Predictive Current Control	50W	93.6%	0.987	15.9%
CCM/DCM Predictive Current Control	50W	93.8%	0.994	7.3%
Adaptive Switching CCM/DCM Current Control	50W	94.6%	0.994	5.9%
Adaptive Frequency CCM/DCM Current Control	50W	94.7%	0.996	5.0%
CCM Predictive Current Control	15W	88.6%	0.950	21.2%
CCM/DCM Predictive Current Control	15W	88.6%	0.933	15.6%
Adaptive Switching CCM/DCM Current Control	15W	91.0%	0.937	10.7%
Adaptive Switching CCM/DCM Current Control	15W	92.5%	0.944	12.0%

Table 4.1: Performance comparison of experimental CCM predictive current controller, CCM/DCM predictive current controller, adaptive switching CCM/DCM current controller, and adaptive frequency CCM/DCM current controller ($v_{ac,rms} = 115V$; $f_s = 80kHz$)(transistor: STP25NM60N; diode: CSD04060).

	Total Equivalent Gate Count
CCM Predictive Current Control	9.2k
CCM/DCM Predictive Current Control	11.0k
Adaptive Switching CCM/DCM Current Control	11.2k
Adaptive Frequency CCM/DCM Current Control	12.1k

Table 4.2: Total equivalent gate count of experimental CCM predictive current controller, CCM/DCM predictive current controller, adaptive switching CCM/DCM current controller, and adaptive frequency CCM/DCM current controller ($v_{ac,rms} = 115\text{V}$; $f_s = 80\text{kHz}$).

Chapter 5

Current Error Estimation

In addition to the dual mode operation over wide load range, the need for current sampling and analog to digital conversion (ADC) is another important issue to be addressed in digital controllers for power factor correction (PFC) rectifiers. For universal input operation, since the duty ratio changes from about 5% to 100%, an ADC with relatively short conversion time is required to obtain the corresponding digital current value. In order to achieve low conversion time, a high speed ADC is required for current sensing. On the other hand, inductor current varies a lot over the line period (T_L) in boost PFC rectifiers. PFC rectifiers process high current at peak of the line voltage and almost no current at the line voltage zero crossings. For wide load range operation, medium to high resolution is necessary for current sensing ADC to achieve low current harmonic distortion. Therefore, high speed and medium resolution ADCs are the common choices for current sensing in digital PFC controllers.

In order to reduce sampling rate of the current sensing, digital boost PFC controllers often sample current once per switching period with precise timing of sampling. It is possible to have some current sensing offset due to the sampling time shift. Besides, when the duty ratio is close to 0% or 100%, current sampling and hold may be affected by the switching noise. Alternatively, sampling on either transistor conduction interval or diode conduction interval is one solution [13,58]. However, continuity in current sensing values between alternative conduction intervals is highly dependent on the sampling timing, which can be affected by the gate drive delay and the transistor turn-on/turn-off delay [58].

In order to achieve a wide load range operated boost PFC rectifier and relieve all of the current sampling issues mentioned above, a new current error estimation approach in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM) is proposed in this chapter. This chapter is organized as following: Sec. 5.1 describes the principle of the new current error estimation approach. A small signal discrete model of the current dynamics based on current error estimation is shown in Sec. 5.2. A low design effort current controller based on current error estimation is introduced in Sec. 5.3. Implementation issues in the digital current controller combining the current error estimation and the adaptive approaches of Chapters 3 and 4 are discussed in Sec. 5.4, followed by experimental results and discussion in Sec. 5.5.

5.1 Principle of Current Error Estimation

To design a digital controller for universal-input boost PFC rectifier over a wide range of loads, a new current error estimation approach in both CCM and DCM is proposed in this chapter. The proposed approach uses a digital to analog converter (DAC) and a single current comparator to measure the timing information, which can indicate the difference between reference current and average inductor current (Fig. 5.1). The hardware of the current error estimation is similar to that of the one bit voltage and current sensing in [59–63]. By using comparator signals, current comparator signal and DCM comparator signal shown in Chapter 3, inductor error current can be estimated and applied in the digital control algorithm, as shown in Fig. 5.1. The current comparator signal (s_L) compares the inductor current (i_L) and the reference current (i_{ref}), where current reference signal is the output of DAC fed from the digital controller.

5.1.1 Current Error Estimation in CCM

The idea of current error estimation in CCM is based on 50% duty ratio of s_L signal when current error is zero. The current error is estimated using the duty ratio of s_L , the inductance value (L) and the input/output voltages (v_g , V_o). Operation waveforms of the current error estimation in CCM are shown in Fig. 5.2.

Figure 5.2: Waveforms illustrating current error estimation in CCM.

As Fig. 5.2 shows, current error (Δi), which is the current difference between i_{ref} and average inductor current over a switching period $\langle i_L \rangle_{T_s}$, is related to the time intervals (ΔT_1 , ΔT_2) and inductor rising and falling slopes,

$$\Delta i = \Delta T_1 \cdot \frac{v_g}{L} = \Delta T_2 \cdot \frac{V_o - v_g}{L}. \quad (5.1)$$

Let the sum of the two time intervals (ΔT_1 , ΔT_2) be ΔT , which is proportional to ΔT_1 , ΔT_2 ,

$$\Delta T = \Delta T_1 \cdot \frac{V_o}{V_o - v_g} = \Delta T_2 \cdot \frac{V_o}{v_g}. \quad (5.2)$$

In CCM, when i_{ref} equals to $\langle i_L \rangle_{T_s}$, ΔT is exactly zero. The sum of s_L logic-low intervals at transistor or diode conduction periods, $T_{L1} + T_{L2}$, equals to one half of the switching period (T_s). Therefore, ΔT is

$$\Delta T = T_{L1} + T_{L2} - \frac{T_s}{2}. \quad (5.3)$$

By combining Eq. 5.1 to Eq. 5.3, in CCM, the current error (e_i) can be estimated using Eq. 5.4, as

$$e_i \approx \Delta i = \left(T_{L1} + T_{L2} - \frac{T_s}{2} \right) \left(\frac{V_o - v_g}{V_o} \right) \left(\frac{v_g}{L} \right). \quad (5.4)$$

5.1.2 Current Error Estimation in DCM

Current error can also be estimated in DCM, as illustrated in Fig. 5.3. Current error (Δi) in DCM is also related to the time intervals (ΔT_1 , ΔT_2) and the inductor rising and falling slopes (Eq. 5.1).

In DCM, the average inductor current $\langle i_L \rangle_{T_s}$ is equal to one half of the peak inductor current $i_{L,peak}$ times the current sensing correction factor (κ),

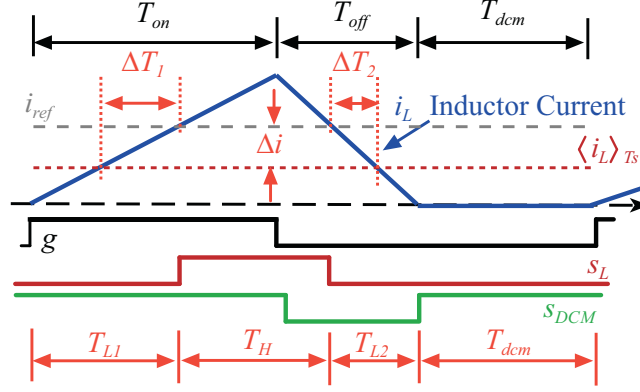


Figure 5.3: Waveforms illustrating current error estimation in DCM.

$$\kappa = \frac{\langle i_L \rangle_{T_s}}{i_{L,peak}/2} = \left(1 - \frac{T_{dcm}}{T_s}\right), \quad (5.5)$$

which has been introduced in Chapter 3.

From Eq. 5.5, the relationship between $i_{L,peak}$ and $\langle i_L \rangle_{T_s}$ can be expressed as a function of the conduction period (T_{cond}), as

$$2\kappa = \frac{\langle i_L \rangle_{T_s}}{i_{L,peak}} = \frac{1}{2} \left(\frac{T_{cond}}{T_s} \right). \quad (5.6)$$

Based on the geometry of the waveforms shown in Fig. 5.3, it is known that desired T_L is proportional to the ratio between the average inductor current and the peak inductor current,

$$\frac{\langle i_L \rangle_{T_s}}{i_{L,peak}} = \frac{1}{T_{cond}} (T_{L1} + T_{L2})_{ref}, \quad (5.7)$$

where $(T_{L1} + T_{L2})_{ref}$ is the desired value of T_L .

From Eq. 5.6 and Eq. 5.7, ΔT can be described as

$$\Delta T = T_{L1} + T_{L2} - (T_{L1} + T_{L2})_{ref} = T_{L1} + T_{L2} - \frac{T_{cond}^2}{2T_s}. \quad (5.8)$$

Therefore, estimated current error (e_i) in DCM can be expressed as.

$$e_i \approx \Delta i = \left(T_{L1} + T_{L2} - \frac{T_{cond}^2}{2T_s} \right) \left(\frac{V_o - v_g}{V_o} \right) \left(\frac{v_g}{L} \right). \quad (5.9)$$

Eq. 5.4 and Eq. 5.9 show that a current reference DAC and two comparators can be used to estimate the current error in both CCM and DCM. Current error estimation in CCM (Eq.5.4) is a special case of estimate in DCM (Eq. 5.9), when T_{cond} is equal to T_s .

5.1.3 Resolution Considerations In Using Current Error Estimation

Current error estimation trades time resolution for current sensing ADC resolution. The relationship between current sensing resolution and time resolution is depended on inductor current ramp up/down slopes, as illustrated in Fig. 5.2. There is a linear relationship between current error (Δi) and time intervals ($\Delta T = \Delta T_1 + \Delta T_2$). Eq. 5.1 can be rewritten as

$$\Delta i = (\Delta T) \left(\frac{v_{eq}}{L} \right), \quad (5.10)$$

where v_{eq} is the equivalent voltage across the inductor to produce corresponding ΔT . The equivalent voltage is

$$v_{eq} = (v_g) \left(\frac{V_o - v_g}{V_o} \right), \quad (5.11)$$

which is always a positive number.

To make the current resolution equal to the time resolution, the following equation has to be valid,

$$\frac{I_{max}}{2^{N_{ADC}}} = \left(\frac{v_{eq}}{L} \right) \left(\frac{T_s}{2^{N_{DPWM}}} \right), \quad (5.12)$$

where N_{ADC} and N_{DPWM} are the number of bits in ADC and DPWM respectively, and I_{max} is maximum possible inductor current at maximum power.

The equivalent number of bits in current sensing (N_{ADC}) can be expressed as

$$N_{ADC} = N_{DPWM} + \log_2 \left[\left(\frac{2 \cdot P_{max}}{V_{M,min}} \right) \left(\frac{1}{T_s} \right) \left(\frac{L}{v_{eq}} \right) \right], \quad (5.13)$$

where P_{max} is the rated power and V_M is line peak voltage.

Eq. 5.13 shows that the current sensing resolution using current error estimation varies with v_g , and the worst case happens when v_g is one half of V_o . Ideally, by selecting large L , the sensing resolution increases. However, due to the small inductor current ripple, interval detecting will be affected by the offset in comparator. This is a tradeoff in selecting the inductor value.

5.2 Current Dynamics Using Current Error Estimation

Current error estimation senses the timing information based on inductor current comparator signal, which is different from the regular discrete-time current feedback system. Small signal discrete-time model of the current dynamics using current error estimation is also different from the regular discrete-time current dynamics discussed in Chapter 3. For the stability consideration and current controller design purpose, the discrete current dynamic model using current error estimation in both CCM and DCM are presented in this section.

5.2.1 Current Dynamics Using Current Error Estimation in CCM

In CCM, operation waveforms related to current error estimation are shown in Fig. 5.4. It is shown that the inductor valley current (i_{Lv}) can be expressed as a function of switching period (T_s) and transistor conduction period (T_{on}), as

$$i_{Lv}[n] = i_{Lv}[n-1] + T_s \cdot \frac{(v_g - V_o)}{L} + T_{on}[n] \cdot \frac{V_o}{L}. \quad (5.14)$$

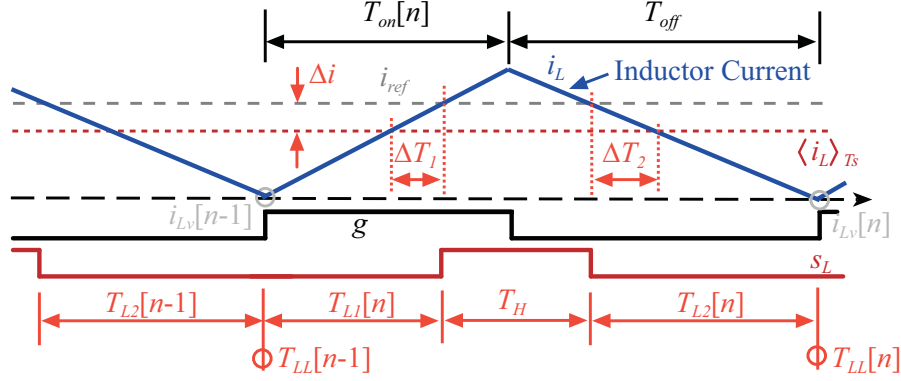


Figure 5.4: Waveforms to illustrate sampling in small signal discrete model in CCM using current error estimation.

i_{Lv} can also be expressed as a function of the s_L logic low period during transistor/diode conduction ($T_{LL} = T_{L1} + T_{L2}$) and T_{L1} , which is part of T_{LL} . The difference equation is

$$i_{Lv}[n] = i_{Lv}[n-1] + T_{LL}[n] \cdot \frac{(v_g - V_o)}{L} + T_{L1}[n] \cdot \frac{V_o}{L}. \quad (5.15)$$

By combining Eq. 5.14 and Eq. 5.15, Eq. 5.16 shows the difference equation, as

$$T_s \cdot (v_g - V_o) + d[n] \cdot T_s \cdot V_o = T_{LL}[n] \cdot (v_g - V_o) + T_{L1}[n] \cdot V_o. \quad (5.16)$$

Applying z-transform to Eq. 5.16, the small signal discrete-time relationship is

$$T_s \cdot (v_g - V_o) + D(z) \cdot T_s \cdot V_o = T_{LL}(z) \cdot (v_g - V_o) + T_{L1}(z) \cdot V_o. \quad (5.17)$$

Since T_{LL} and T_{L1} are depended variables, their relationship can be expressed as

$$(T_{LL}[n-1] - T_{L1}[n-1]) (V_o - v_g) = T_{L1}[n] \cdot v_g. \quad (5.18)$$

Applying z-transform to Eq. 5.18, the small signal discrete-time relationship between T_{LL} and T_{L1} can be found as

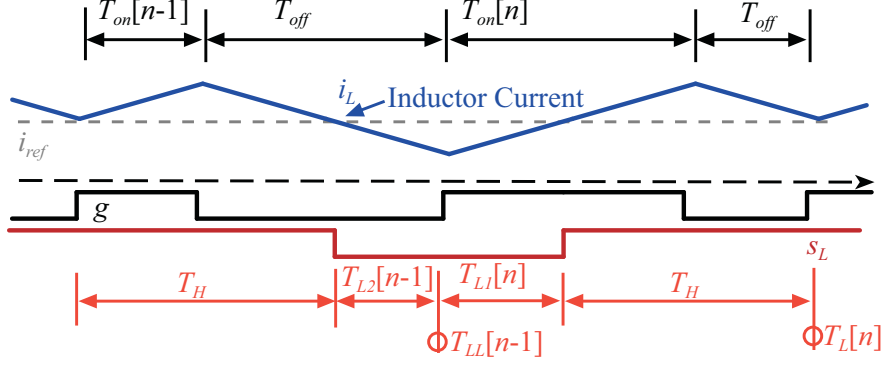


Figure 5.5: Waveforms to illustrate zero effect in small signal discrete model in CCM using current error estimation.

$$(V_o - v_g) \cdot T_{LL}(z) = [v_g \cdot z + (V_o - v_g)] \cdot T_{L1}(z). \quad (5.19)$$

From Eq. 5.17 and Eq. 5.19, small signal discrete transfer function from duty ratio d to T_{LL} in CCM can be expressed as

$$\frac{T_{LL}(z)}{D(z)} = \frac{V_o}{(v_g - V_o)} \cdot T_s \cdot \frac{\left[z + \frac{(V_o - v_g)}{v_g} \right]}{[z - 1]}. \quad (5.20)$$

The small signal discrete-time model changes the gain based on the slopes of the transistor/diode turned-on intervals. The small signal discrete transfer function from d to T_{LL} has the maximum gain when input voltage (v_g) is exactly one half of the output voltage (V_o). Eq. 5.20 also shows an integration effect, which is the same as the average model from d to i_L . However, d to T_{LL} transfer function, Eq. 5.20, has an extra zero at high frequency. Fig. 5.5 illustrates an example of the zero effect, which illustrates the period doubling in duty ratio.

5.2.2 Current Dynamics Using Current Error Estimation in DCM

In DCM, on the other hand, T_{LL} becomes a constant with duty ratio perturbation, as illustrated by the waveforms in Fig. 5.6. The only term affected by duty ratio perturbation is

the conduction interval (T_{cond}) and the discontinuous conduction interval (T_{dcm}). The relationship between T_{dcm} and d is

$$T_s - T_{dcm}[n] = d[n] \cdot T_s \cdot \frac{V_o}{(V_o - v_g)}. \quad (5.21)$$

Applying z-transform to Eq. 5.21, the small signal discrete-time transfer function from d to T_{dcm} is

$$\frac{T_{dcm}(z)}{D(z)} = -T_s \cdot \frac{V_o}{(V_o - v_g)}. \quad (5.22)$$

d to T_{dcm} transfer function forms a sample gain relationship which varies with rectified input voltage v_g . When rectified line voltage v_g is close to output voltage V_o , there is a large gain from d to T_{dcm} .

5.3 Current Controller Design Based on Current Error Estimation

The proposed digital controller using current error estimation is based on the predictive current mode control, which is an average current mode controller with an additional feed-forward term. The block diagram of the proposed current controller is shown in Fig. 5.7. A proportional and integral (PI) current compensator to reduce estimated current error (e_i) and a feed-forward term are added together to form a simple current controller. A set of the operation equations is:

$$T_{on}[n] = T_{on}[n-1] + \alpha \cdot e_i[n-1] \cdot T_s + \beta \cdot \alpha \cdot e_i[n-2] \cdot T_s + T_{on,ff}, \quad (5.23)$$

$$\alpha \cdot e_i[n] = \left(T_{LL}[n] - \frac{T_{cond}^2[n]}{2T_s} \right) \left(\frac{V_o - v_g}{V_o} \right) \left(\frac{v_g}{V_o} \right) \left(\frac{1}{T_s} \right), \quad (5.24)$$

$$\alpha = \frac{L}{V_o T_s}, \quad (5.25)$$

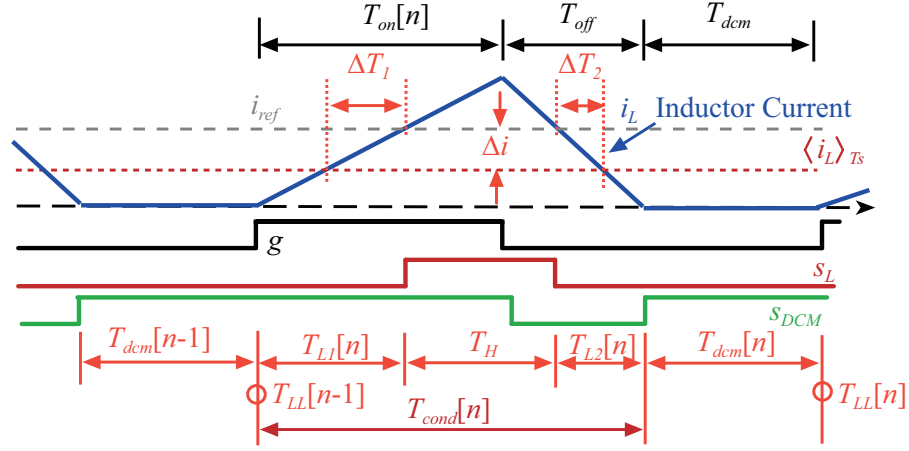


Figure 5.6: Waveforms to illustrate sampling in small signal discrete model in DCM using current error estimation.

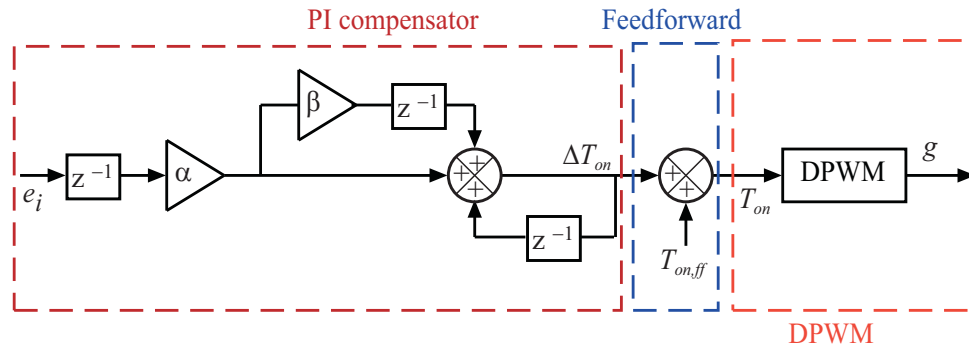


Figure 5.7: Block diagram of current controller (using current error estimation).

where α and β are the PI compensator parameters described in Chapter 3.

Note that current control rule (Eq. 5.23 and Eq. 5.24) does not require precise inductor value (L) estimation. The proposed current controller rule requires voltage information (V_o and v_g) and timing information (T_L , T_s and T_{cond}) only, which is different from the usual average current mode control. Therefore, the proposed current control rules using current error estimation (Eq. 5.29 and Eq. 5.30) form a current controller that requires low design effort and has improved robustness.

From the control rules, in CCM, T_{cond} is always equal to switching period (T_s). As a result, small signal discrete transfer function of the current controller in CCM (G_{icz_CCM}) can be expressed as Eq. 5.26. Applying G_{icz_CCM} , the current loop bandwidth in CCM is fixed and is independent of the inductor value, as

$$G_{icz_CCM}(z) = \frac{D(z)}{T_L(z)} = \left(\frac{V_o - v_g}{V_o} \right) \left(\frac{v_g}{V_o} \right) \left(\frac{1}{T_s} \right) \frac{(z + \beta)}{z(z - 1)}. \quad (5.26)$$

In DCM, assuming the current reference (i_{ref}) is a constant over the entire switching period, T_L is always a constant. Eq. 5.24 is a function of discontinuous conduction period (T_{dcm}), as

$$\alpha \cdot e_i[n] = \left[T_L - \frac{(T_s - T_{dcm}[n])^2}{2T_s} \right] \left(\frac{V_o - v_g}{V_o} \right) \left(\frac{v_g}{V_o} \right) \left(\frac{1}{T_s} \right). \quad (5.27)$$

Neglecting the higher order terms in Eq. 5.27, small signal discrete transfer function of the current controller in DCM (G_{icz_DCM}) can be expressed as

$$G_{icz_DCM}(z) = \frac{D(z)}{T_{dcm}(z)} = \left(\frac{V_o - v_g}{V_o} \right) \left(\frac{v_g}{V_o} \right) \left(\frac{1}{T_s} \right) \frac{(z + \beta)}{z(z - 1)}. \quad (5.28)$$

From Eq. 5.20 and Eq. 5.26 in CCM and Eq. 5.22 and Eq. 5.28 in DCM, the corresponding current loop gain magnitudes and phase responses for CCM and DCM operations are shown in Fig. 5.8. As mentioned in Chapter 3, it can be observed that the gain and the cross-over frequency are much lower in DCM than that in CCM.

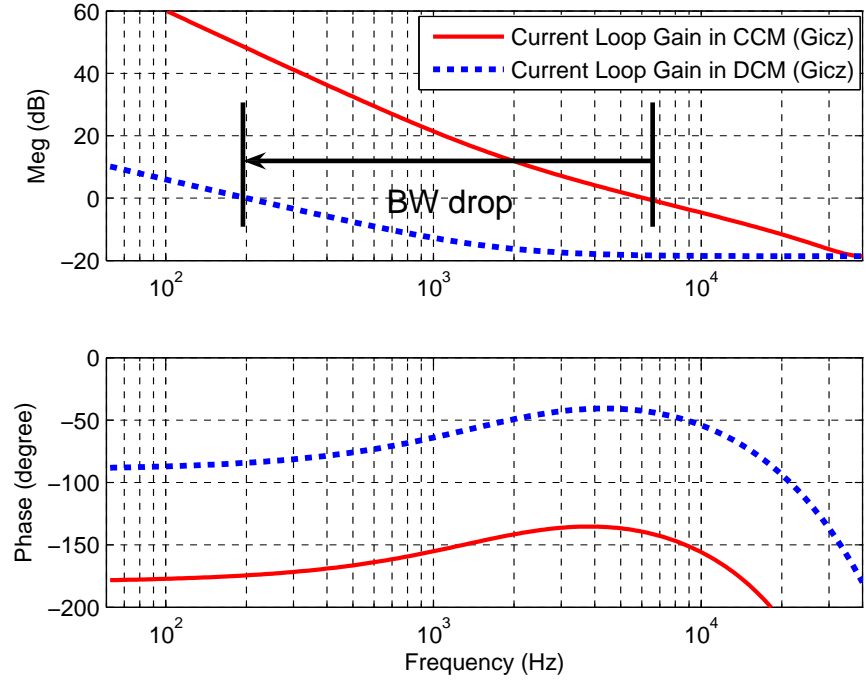


Figure 5.8: Current loop dynamics with current loop compensator G_{icz} using current error estimation in CCM (200 W) and DCM (80 W) ($f_s = 80$ kHz; $L = 0.5$ mH; $v_g = 100$ V).

The modified compensator gain in Chapter 3 requires both the inductor and the load information. In order to simplify the current loop and achieve low design effort in current controller, a modified PI compensator is applied to maintain relatively high current loop bandwidth. The compensator parameter, β , in Eq. 5.29 is adjusted based on the operating mode, CCM or DCM. In DCM, the compensator gain β_{dcm} is set to be zero to increase bandwidth in DCM. Fig. 5.9 shows that the modification results in much improved bandwidth of the current control loop.

5.4 Adaptive CCM/DCM Controller Based on Current Error Estimation

In order to operate the boost PFC over a wide range of loads and to eliminate sampling issues on current sensing ADC, the proposed digital controller combines the current error estimation and the adaptive switching for DCM operation. The controller takes advantage of two slow ADC sensing information (v_g , V_o) and two fast comparator information (s_L , s_{DCM}) to shape inductor current, and combines the adaptive CCM/DCM approach (Chapter 3) to increase light load efficiency and current error estimation (Sec. 5.1) to relieve the current sensing ADC requirement. This section shows the implementation of the proposed digital controller.

The state machine of the proposed current controller is built on a digital counter (*counter*) based trailing edge digital pulse width modulator (DPWM), which is implemented using field programmable gate array (FPGA) with 100 MHz clock frequency. The switching period starts from transistor turned-on state (S_{Qon}); after the transistor is turned off, the system is in the diode conduction state (S_{Don}). If the DCM comparator signal (s_{DCM}) does not flip on before the end of the nominal operation period (T_s), the system operates in CCM and starts another switching period right at the end of T_s . On the other hand, if s_{DCM} flips on before the end of T_s , the system enters state S_{VxL} and starts DCM mode. Depending on s_{DCM} , the state machine toggles between S_{VxL} and S_{VxH} to measure T_{osc} . Before starting another switching period, the system waits for one half of T_{osc} to achieve valley voltage switching at minimum v_{ds} , which extends the actual switching period to be T_{sw} . Due to the addition of the adaptive switching, the whole set of the current control rules are modified from Eq. 5.29- Eq. 5.32, and are shown as the follows:

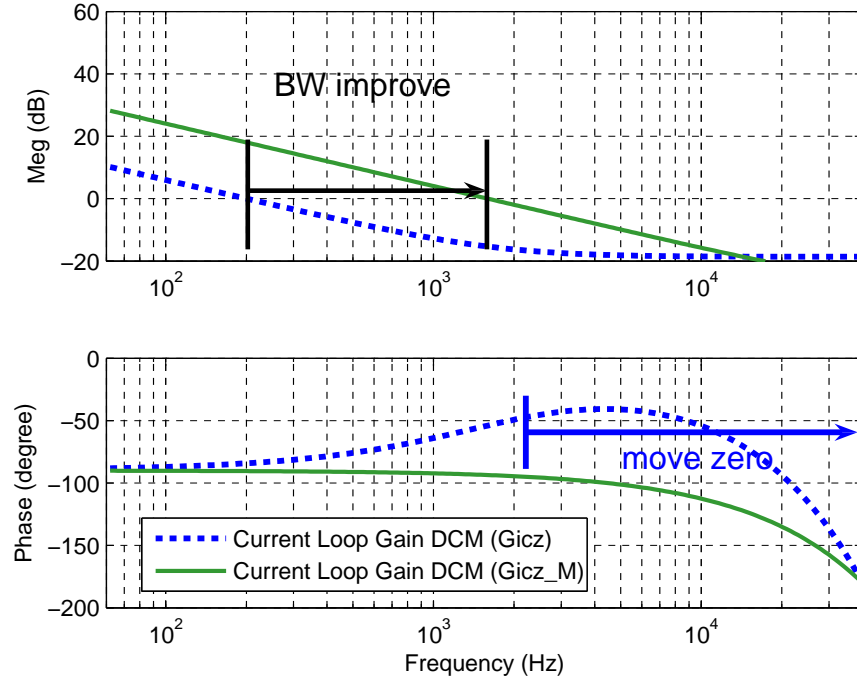


Figure 5.9: Current loop dynamics with current loop compensator G_{icz} and modified compensator G_{icz_M} using current error estimation in DCM (80 W) ($f_s = 80$ kHz; $L = 0.5$ mH; $v_g = 100$ V).

$$T_{on}[n] = T_{on}[n-1] + \alpha \cdot e_i[n-1] \cdot T_s + \beta \cdot \alpha \cdot e_i[n-2] \cdot T_s + T_{on,ff}, \quad (5.29)$$

$$\alpha \cdot e_i[n] = \left(T_{LL}[n] - \frac{T_{cond}^2[n]}{2T_s} \right) \left(\frac{V_o - v_g}{V_o} \right) \left(\frac{v_g}{V_o} \right) \left(\frac{1}{T_s} \right), \quad (5.30)$$

$$T_{on,ff} = \min \left[\left(1 - \frac{v_g}{V_o} \right) \cdot T_s, \sqrt{\left(1 - \frac{v_g}{V_o} \right) \cdot \frac{2Lu}{T_s}} \right], \quad (5.31)$$

$$\beta = \begin{cases} -7/8 & CCM \\ 0 & DCM \end{cases}. \quad (5.32)$$

There are some possible fault conditions. First, when inductor current is away from the reference current, the controller is out of the linear region. It makes the current error estimation inaccurate and slows down the current tracking. To enforce the controller to operate in linear region, the system sets one limitation, as illustrated in Fig. 5.10. The state machine will not start another switching period until the inductor current i_L is lower than the reference current i_{ref} . On the other hand, due to the control of the transistor turn-on timing, there is no guarantee that the inductor current will pass the reference current during the transistor turn-on interval. Nevertheless, keeping relatively high bandwidth and proper current ripple usually results in linear operation of the controller. However, around input voltage zero-crossings, close-to-one duty ratio is expected. It is possible that the transistor turn-off noise accidentally flips s_L low and sets the current loop out of the linear region. Blinding s_L to have multiple low states prevents this fault condition around the line voltage zero crossing.

5.5 Results and discussion

The same boost PFC power stage designed as in Chapter 3 and Chapter 4, a 300W boost PFC rectifier ($f_s \approx 80$ kHz; $L = 0.5$ mH; $C = 220$ μ H), is built as shown in Fig. 5.1, using FPGA

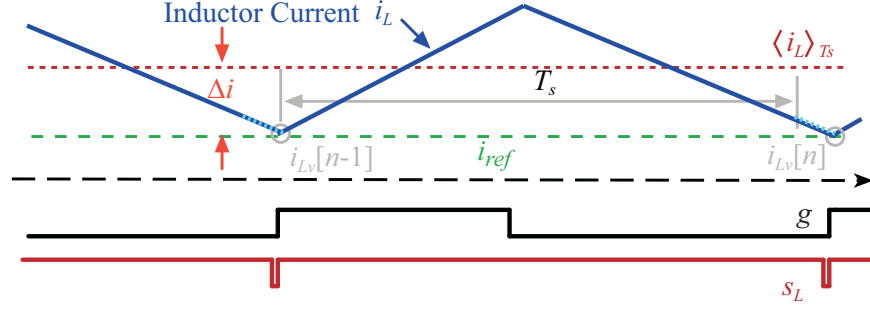


Figure 5.10: Waveforms illustrating a fault condition in current error estimation.

development platform to implement the digital controller with 100 MHz clock as time resolution. The experimental setup is shown in Fig. 5.11.

Using the current error estimation, proposed digital current controller regulates the inductor current by having s_L with 50% duty ratio in CCM operation, as illustrated in Fig. 5.12. In DCM operation, the proposed digital current controller estimates current error using the comparator signals, s_L and s_{DCM} , and regulates the inductor current. Fig. 5.13 shows a functional operation of the current error estimation in DCM with the adaptive switching technique.

At heavy load, when the converter operated in CCM over the entire line period, the current controller using current error estimation operates at constant frequency and achieves low current harmonic distortion (Fig. 5.14).

At medium load, when the converter operates in mixed mode (CCM and DCM), there is more current distortion (Fig. 5.15 at low line voltage; Fig. 5.16 at high line voltage). The current distortion is caused by the mode detection error, since the DCM detection comparator is using the voltage mode instead of the current mode detection, DCM detection comparator is not able to decide the correct operation mode around the light DCM operating mode.

At light load, when the converter operates in DCM over the entire line period, due to the modified current compensator, the current loop still has relatively high bandwidth. Current distortion happens around input voltage zero-crossing (Fig. 5.17 at low line voltage; Fig. 5.18 at high line voltage).



Figure 5.11: Evaluation board and experiment setup (current error estimation).

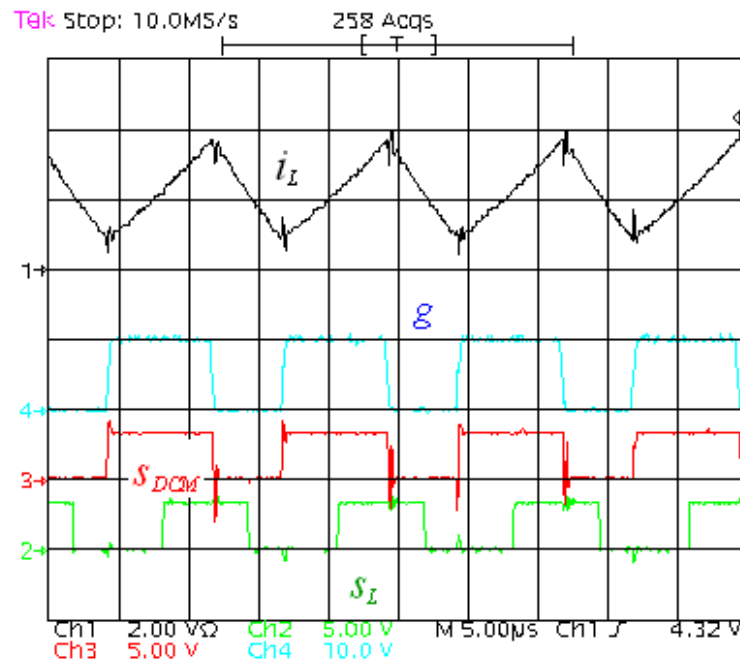


Figure 5.12: Experimental boost PFC converter waveforms in CCM using current error estimation, inductor current i_L , inductor current comparator signal s_L , gate drive signal g and DCM comparator signal s_{DCM} ($f_s = 80$ kHz).

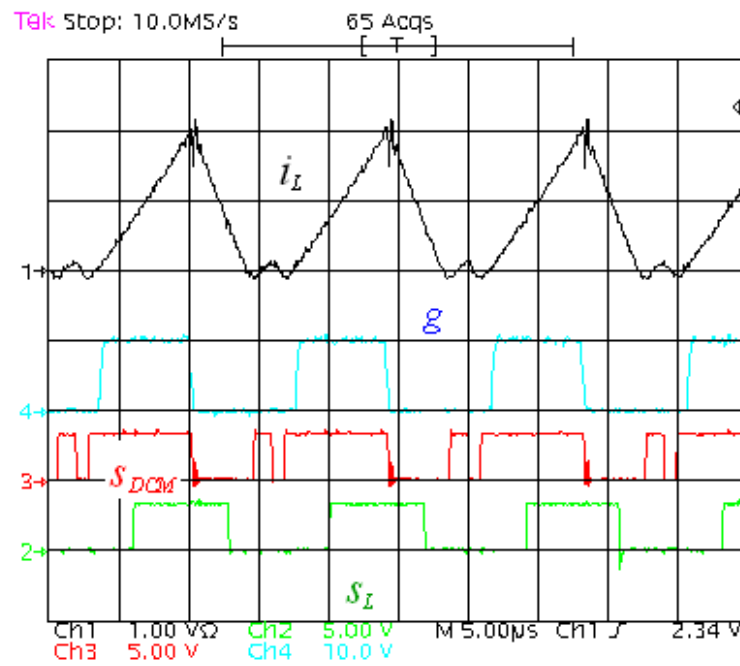


Figure 5.13: Experimental boost PFC converter waveforms in CCM using current error estimation, inductor current i_L , inductor current comparator signal s_L , gate drive signal g and DCM comparator signal s_{DCM} ($f_s \approx 80$ kHz).

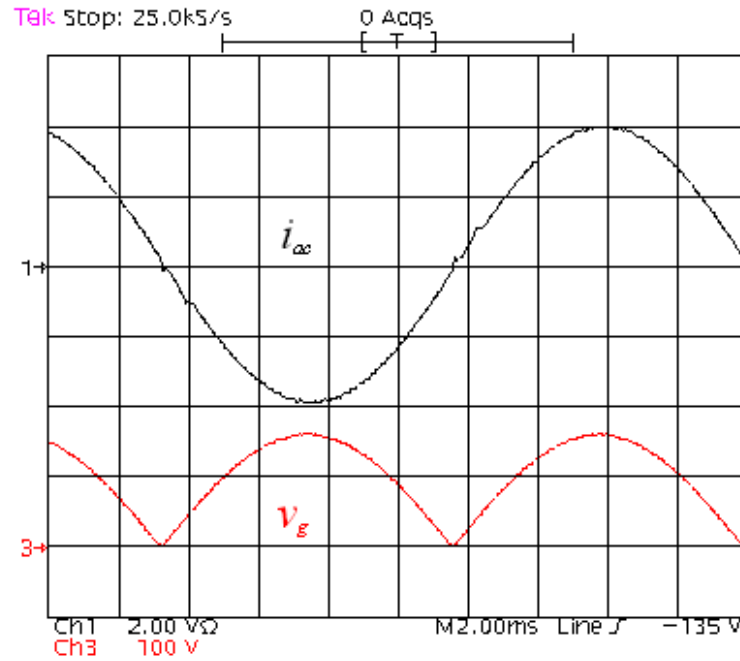


Figure 5.14: Experimental boost PFC converter waveforms, rectified line voltage v_g and line current i_{ac} , adaptive switching CCM/DCM controller using current error estimation ($f_s = 80$ kHz; 300 W).

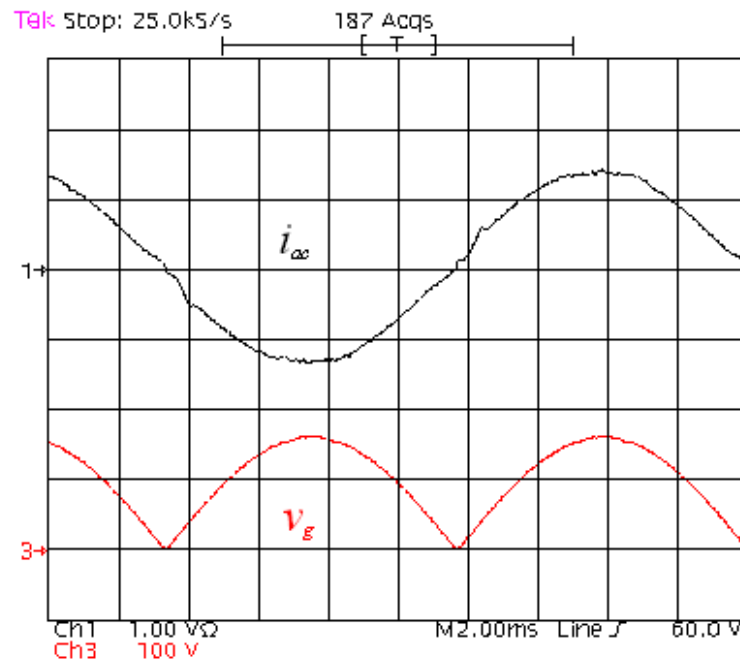


Figure 5.15: Experimental boost PFC converter waveforms, rectified line voltage v_g and line current i_{ac} , adaptive switching CCM/DCM controller using current error estimation ($f_s \approx 80$ kHz; 100 W).

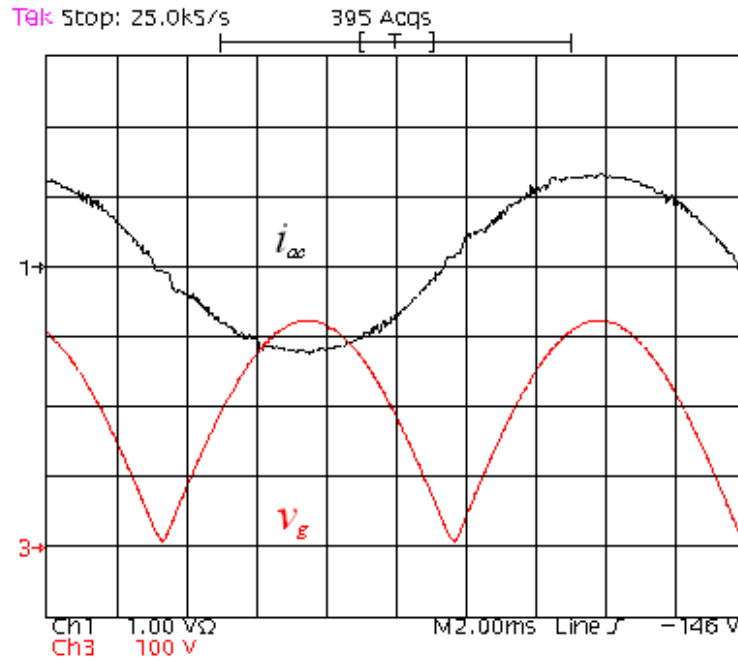


Figure 5.16: Experimental boost PFC converter waveforms, rectified line voltage v_g and line current i_{ac} , adaptive switching CCM/DCM controller using current error estimation ($f_s \approx 80$ kHz; 200 W).

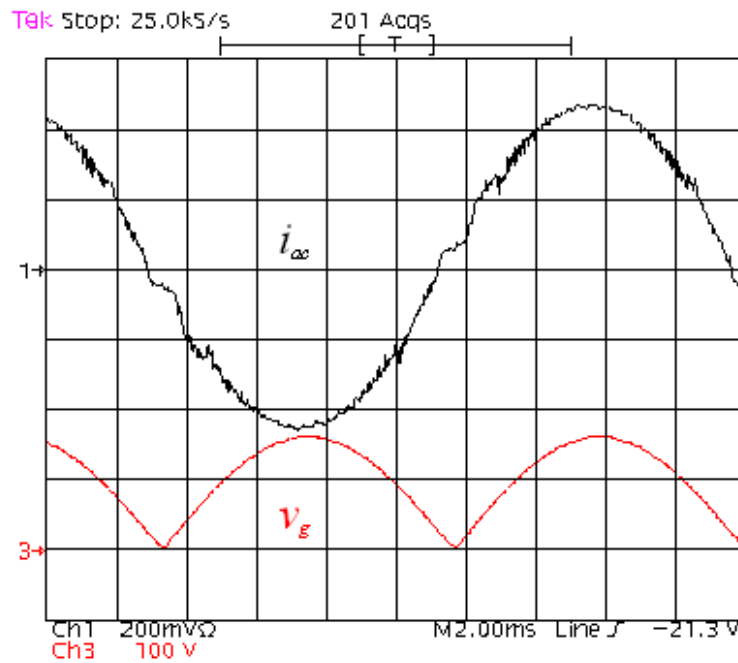


Figure 5.17: Experimental boost PFC converter waveforms, rectified line voltage v_g and line current i_{ac} , adaptive switching CCM/DCM controller using current error estimation ($f_s \approx 80$ kHz; 30 W).

At very light load, the conduction period (T_{cond}) shrinks, while the clock resolution (10 ns) is still the same. Therefore, the error of the current error estimation approach grows, which results in increased current distortion (Fig. 5.19).

Fig. 5.20 illustrates the total harmonic distortion (THD) performance of the adaptive switching CCM/DCM current controller using current error estimation at both high line and low line input voltages. The corresponding high efficiency over wide load range is shown in Fig. 5.21.

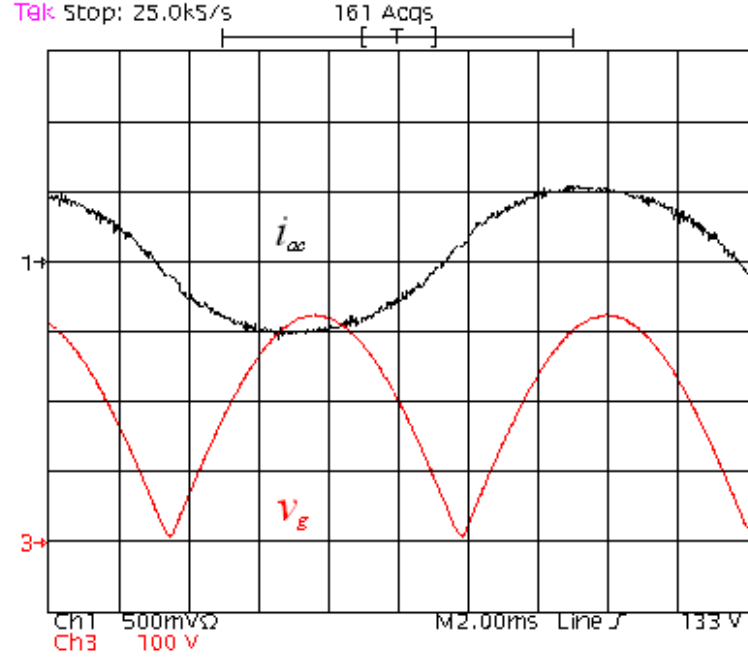


Figure 5.18: Experimental boost PFC converter waveforms, rectified line voltage v_g and line current i_{ac} , adaptive switching CCM/DCM controller using current error estimation ($f_s \approx 80$ kHz; 75 W).

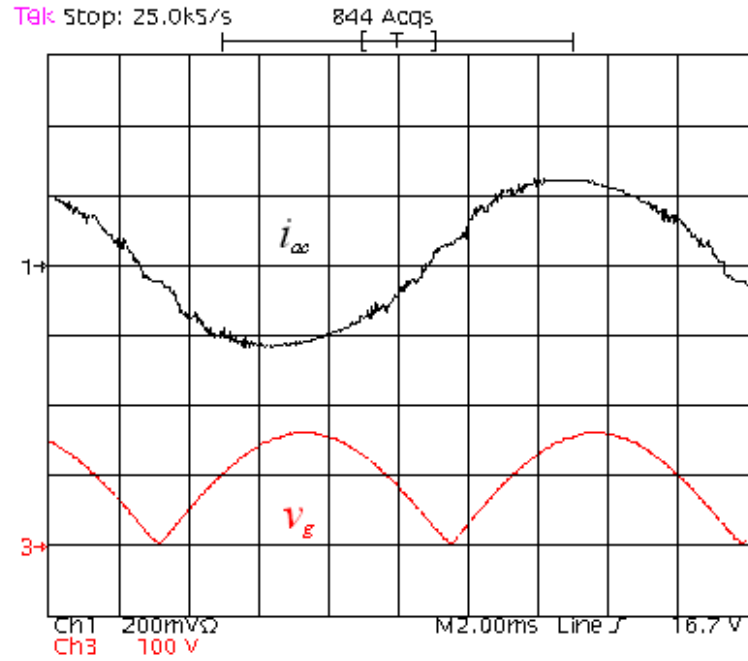


Figure 5.19: Experimental boost PFC converter waveforms, rectified line voltage v_g and line current i_{ac} , adaptive switching CCM/DCM controller using current error estimation ($f_s \approx 80$ kHz; 15 W).

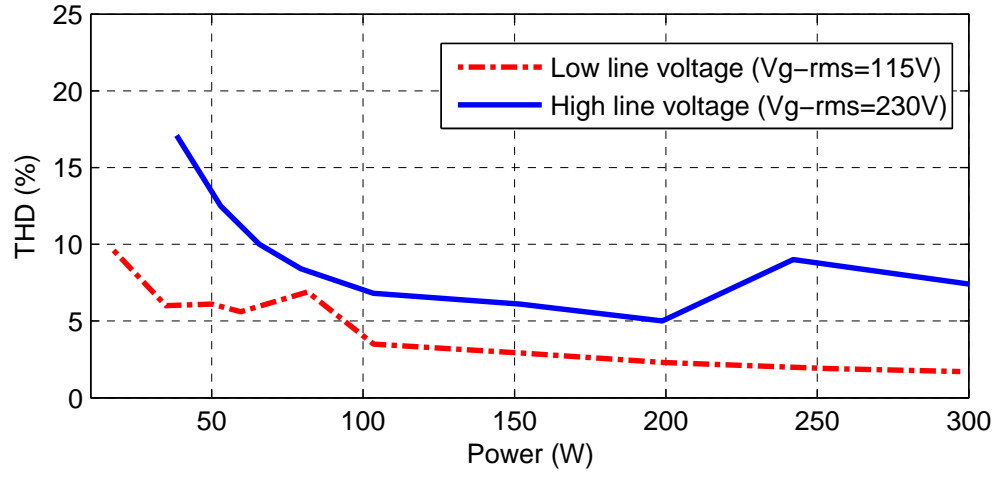


Figure 5.20: Current harmonic distortion using adaptive switching CCM/DCM control with current error estimation ($f_s \approx 80$ kHz).

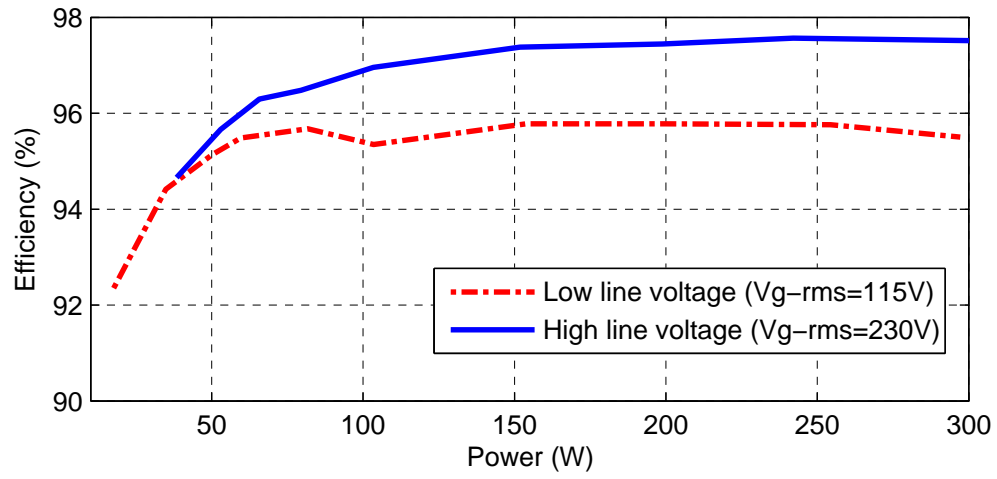


Figure 5.21: Measured efficiency using adaptive switching CCM/DCM control with current error estimation ($f_s \approx 80$ kHz).

Chapter 6

Passive Power Sharing in Interleaved Boost PFC

In order to increase power processing capability, paralleling of phase interleaved modules has been developed in DC-DC converters [64]. By applying phase interleaving among converter modules, the overall inductor current ripple is reduced. Phase interleaved converters with identical converter modules achieves the lowest overall current ripple without increasing inductor size or increasing switching frequency. Fig. 6.1 shows an example of a two-phase buck converter; phase interleaved operation minimizes output voltage ripple and reduces the size of the output capacitors [64].

Paralleling of phase interleaved modules has been adopted in power factor correction (PFC) rectifiers to increase power system modularity [38–40, 65–77]. In order to extend power range, this chapter focuses on digital control for interleaved boost PFC rectifiers. Proposed controller combines passive power sharing approach and adaptive approaches in interleaved boost PFC rectifiers. This chapter starts from an introduction of interleaved boost PFC rectifiers in Sec. 6.1. Issues related to active power sharing approach and passive power sharing approach are discussed in Sec. 6.2. Sec. 6.3 discusses efficiency improvement and current mismatch in the passive power sharing approach. It is followed by an introduction of a new over current protection in Sec. 6.4. Sec. 6.5 discusses issues related to light load efficiency improvements, including phase interleaving and phase shedding. The final section shows experiment results.

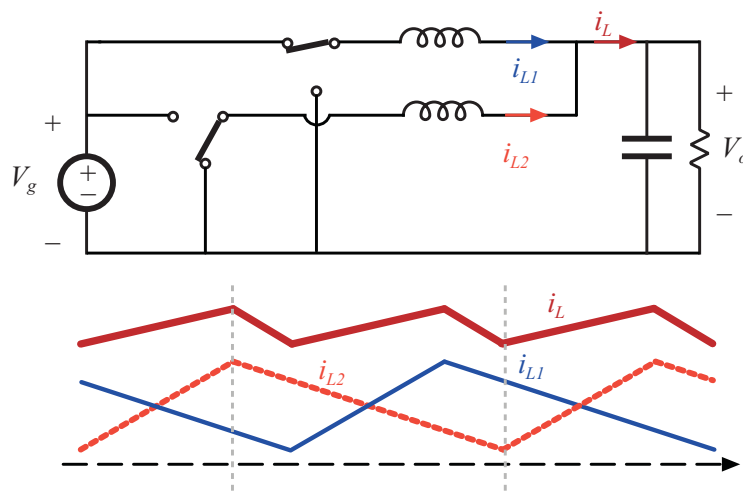


Figure 6.1: Circuit schematics and waveforms of two-phase interleaved buck converter.

6.1 Introduction of Interleaved Boost PFC Rectifiers

Parallelling power converter modules has been developed in DC-DC converters. Multiple modules stack up the power level without changing the selected components and power stage design. Phase-interleaved operation reduces the inductor current ripple or the capacitance size. Voltage regulation module (VRM) in microprocessor power supplies is one of the important applications for multiple modules. For AC-DC rectifiers, interleaved PFC rectifiers starts from the idea of reducing overall inductor current ripple and input filter size. It is originally designed for multiple phase-shifted boost PFC modules operated in discontinuous conduction mode (DCM) [38]. An interleaved boost PFC rectifier, which is operated in continuous conduction mode (CCM), uses two current loops to shape overall inductor current and to achieve current sharing [40]. Furthermore, attention has been given to transition mode (TM) interleaved boost PFC rectifiers [39, 65, 68–71, 75, 76]. Due to the varying frequency operation in TM PFC rectifiers, different types of phase latch control strategies are applied to keep converter modules phase-interleaved.

Recently, digital controllers, which can easily build precise phase interleaving, have been developed in interleaved boost PFC rectifiers to increase system power modularity [66, 67]. Digital controllers can easily add some other extra features, such as phase shedding, without much extra cost [67].

It can be concluded that interleaved boost PFC rectifiers offer a number of benefits. They reduce the overall inductor current ripple without increasing inductor value or switching frequency; they increase power level without changing component selection. However, there are also some drawbacks of interleaved boost PFC rectifiers. The total number of components increases. It becomes more difficult to sense inductor current and to design the pulse width modulator (PWM).

6.2 Active Power Sharing and Passive Power Sharing

Power sharing becomes an issue in parallel converter modules when they are operated in CCM. Different power sharing techniques have been developed in past years. In the approaches

reported so far, power sharing among the paralleled modules operating in CCM has been based on active current sharing control that requires individual current sensing in each module, as shown in a two-phase example in Fig. 6.2.

However, since the modules share a common ground terminal, typically at the negative terminal of the output filter capacitor, and they are all supplied from the same ac line input voltage, current sensing of the separated inductor current values is not available. Generally, two current sensing transformers are applied together with peak current mode control, which results in some current distortion around medium to light load operation [73]. Another common approach is to sense the total inductor current based on input-side sensing resistance, and to add an extra current sharing control loop and extra current sensing on the switch or the diode legs, as shown in Fig. 6.3 [66, 67]. These active power sharing approaches either require extra current sensing or compromise current distortion.

An alternative, simpler approach based on passive power sharing is proposed here. It uses only one current sensing circuit (as shown in Fig. 6.4) and a digital controller driving the power MOSFETs with phase shifted control signals having identical duty ratios. Such passive power sharing approach has earlier been proposed for multi-phase DC-DC microprocessor power supplies [78], where it was shown to yield minimum overall conduction losses and improved efficiency (at heavy loads) at the expense of unequal distribution of currents among the modules. The passive power sharing approach can only be precisely applied using digital control techniques to optimize efficiency for heavy loads; other approaches are applied to extend high efficiency operation to light load, such as phase shedding and adaptive approaches discussed in previous chapters [79].

A discussion of efficiency and current mismatch tradeoffs for passive power sharing in multi-phase PFC rectifiers such as the two-phase example shown in Fig. 6.4, is given in the next section.

6.3 Efficiency Improvement and Current Mismatch in Passive Power Sharing

A digital controller can produce perfectly matched phase shifted control signals for each module. This property has enabled effective passive current sharing in multi-phase DC-DC con-

The diagram illustrates a power electronic system with a digital control loop. The power stage consists of an AC input v_{ac} and current i_{ac} passing through a bridge rectifier. The output is filtered by an LC network with inductors L_1 and L_2 . The system uses two MOSFETs (Q_1, Q_2) and two diodes (D_1, D_2) in a half-bridge configuration, with a DC-link capacitor C and a load resistor R . The output voltage is V_o and the gate voltage is v_g . The digital controller, shown in a dashed box, receives feedback signals i_L , i_{Q2} , i_{Q1} , V_o , and v_g via ADCs. It processes these signals through a Current Sharing Controller, a Current Controller, and a Voltage Controller to generate reference signals i_{ref} and u . These references are then used by DPWM blocks to produce the gate drive signals for the MOSFETs.

Figure 6.3: Digital interleaved PFC rectifier with active power sharing (two-loop approach) (a two-phase example).

verters [78]. This section examines the outcomes in terms of conduction losses and current mismatch of the passive power sharing approach when the paralleled PFC modules are operated with identical (but phase shifted) switch control signals.

6.3.1 Reduction of Conduction Losses Due to Passive Power Sharing

An ideal single-phase PFC presents a resistive load to the ac line [8]. As shown in Fig. 6.5, a two-phase PFC rectifier is modeled as two emulated resistances (R_{e1} , R_{e2}) on the input side with corresponding controlled power sources P_{ac1} and P_{ac2} , respectively. To simplify the analysis of passive power sharing, conduction losses are approximately modeled as equivalent series resistances R_{Leq1} and R_{Leq2} . Furthermore, the simplified analysis assumes that the inductors are well matched, $L_1 = L_2$.

In CCM operation, under small ripple assumption and $R_{Leq} \ll R_e$, the conduction loss (P_{cond}) can be found as

$$P_{cond} \approx \left(\frac{1}{R_{e1}^2} R_{Leq1} + \frac{1}{R_{e2}^2} R_{Leq2} \right) \cdot V_{ac,rms}^2, \quad (6.1)$$

where $V_{ac,rms}$ is the root-mean-square (RMS) value of the input ac line voltage. It follows that the conduction loss (Eq. 6.1) is minimized if the PFC module emulated resistances satisfy the following condition:

$$\frac{R_{e1}}{R_{e2}} = \frac{R_{Leq1}}{R_{Leq2}}. \quad (6.2)$$

In Fig. 6.6, the normalized conduction loss, which is the conduction loss with respect to the minimum conduction loss over different R_e and R_{Leq} ratios, illustrates how the minimum conduction loss occurs when Eq. 6.2 is satisfied.

In multi-phase PFC rectifiers with active equal power sharing, current controllers for each module are implemented to make the current split evenly among the modules. With evenly shared

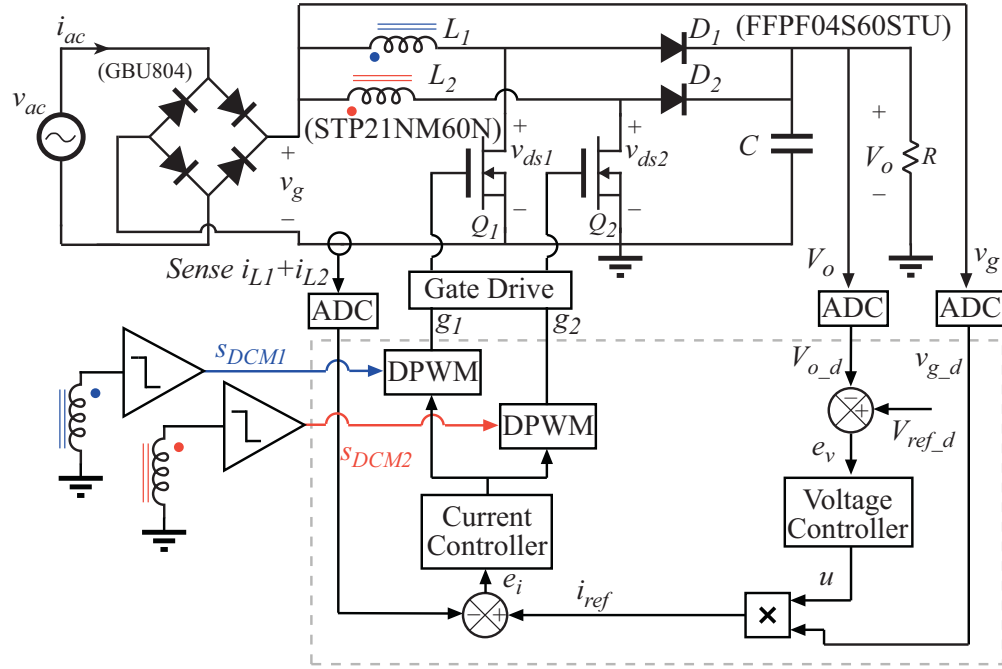


Figure 6.4: Digital interleaved PFC rectifier with passive power sharing (a two-phase example).

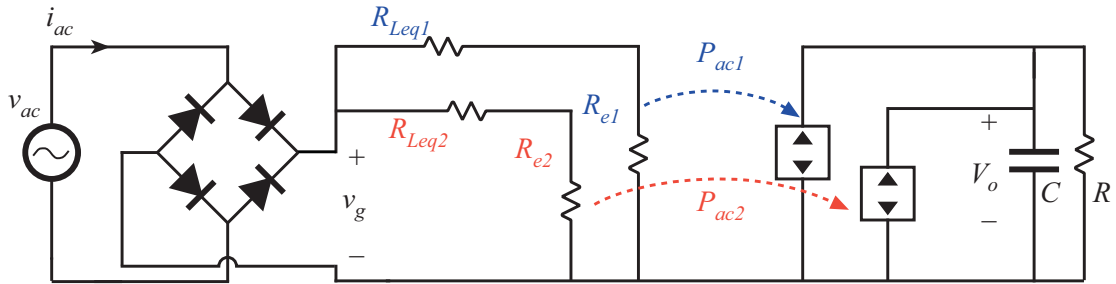


Figure 6.5: Averaged equivalent circuit model of a two-phase boost PFC rectifier, including conduction loss equivalent resistance (R_{Leq1} , R_{Leq2}).

power, the emulated resistances are the same for all modules, $R_{e1} = R_{e2}$. As a result, in the presence of conduction loss mismatches ($R_{Leq1} \neq R_{Leq2}$), equal current sharing does not achieve minimum conduction loss. If the controller drives the power switches with identical duty ratios, while controlling the total input current, it can be shown that the resulting emulated resistances meet Eq. 6.2, which means that the passive power sharing approach minimizes the total conduction losses. A more detailed analysis can be performed based on the models averaged over a switching period T_s , as shown in Fig. 6.7.

In the PFC rectifier with active power sharing, each phase shares equal current (Fig. 6.7(a)). Assuming the inductor values are the same in all phases, and taking into account only conduction losses, overall efficiency of the PFC rectifier with active power sharing can be found by integrating the power loss over the line period, as

$$\eta_{active} = 1 - \frac{R_{Leq}}{2R_e}, \quad (6.3)$$

where $R_{Leq} = (R_{Leq1} + R_{Leq2})/2$ is the nominal equivalent series resistance, and R_e is the total emulated resistance.

In the passive power sharing PFC rectifier, each phase operates at the same duty ratio (Fig. 6.7(b)). Assuming the inductor values are the same in all phases and that the time constant of the inductor ($\tau_L = L/R_{Leq}$) is much shorter than one half of the line period (T_L), overall efficiency of the passive power sharing PFC rectifier becomes a function of the equivalent series resistance mismatch ($\Delta R_{Leq} = |R_{Leq1} - R_{Leq2}|$), as

$$\eta_{active} = 1 - \frac{R_L}{2R_e} + \frac{\Delta R_{Leq}^2}{8R_e R_{Leq}}. \quad (6.4)$$

From Eq. 6.3 and Eq. 6.4, the reduction in conduction loss by passive power sharing is shown in Fig. 6.8 as a function of the relative R_{Leq} mismatch $\Delta R_L/R_{Leq}$. One may note that, although the reduction in conduction losses due to passive power sharing is relatively small, the approach

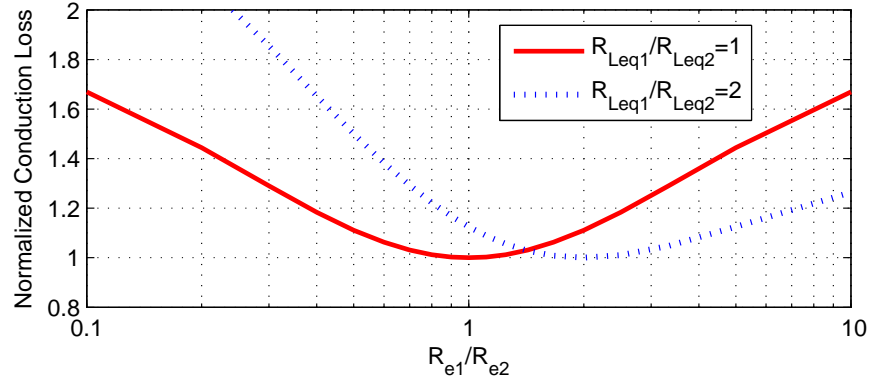
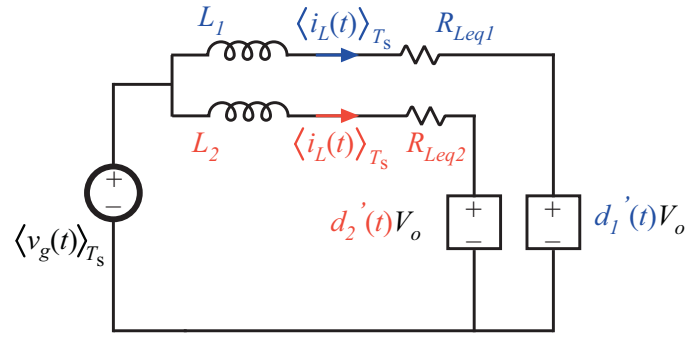
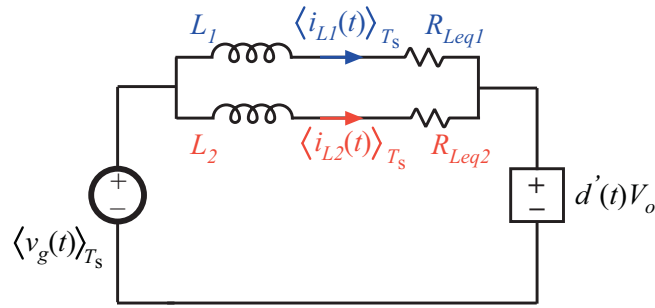


Figure 6.6: Normalized conduction loss with R_e and R_{Leq} mismatch.



(a) Active power sharing



(b) Passive power sharing

Figure 6.7: Averaged switch model in boost PFC rectifier for current loop with R_e and R_{Leq} mismatch (two-phase example).

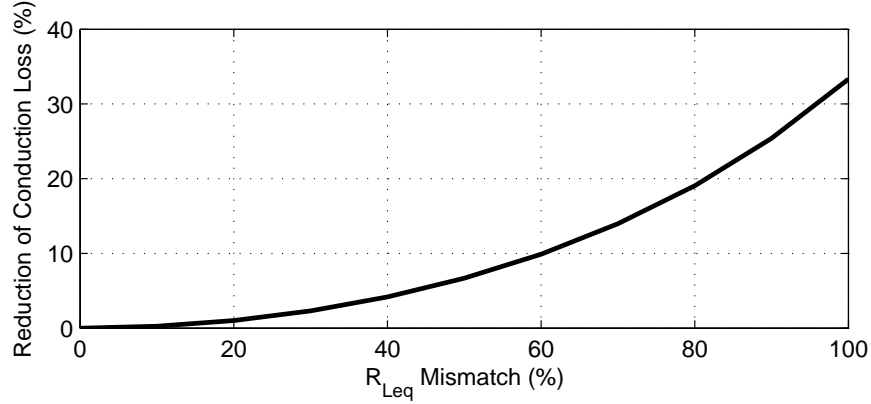


Figure 6.8: Reduction of conduction loss using passive power sharing in the two-phase boost PFC rectifier in CCM.

can result in efficiency improvements at heavy loads where conduction losses dominate. A detailed analysis of converter efficiency with active and passive power sharing is presented in Appendix B.

6.3.2 Current Mismatch Due to Passive Power Sharing

In the presence of component mismatches, passive power sharing helps to reduce conduction losses. A disadvantage is that each phase processes different amount of power, and the resulting current mismatch increases the current stresses on the components. With passive power sharing, the current mismatch can be related to a mismatch in the equivalent series resistances, a mismatch in the inductance values, and the phase shift between the PFC modules. This section presents an approximate analysis of each of these three effects separately. From the model in Fig. 6.7(b), considering the R_{Leq} mismatch only, the maximum relative current difference can be found as

$$\max[\Delta i_L] \approx \frac{V_M}{2R_e} \cdot \frac{\Delta R_{Leq}}{R_{Leq}}, \quad (6.5)$$

where V_M is the peak ac line voltage. The current-mismatch penalty is illustrated in Fig. 6.9, which shows the maximum current mismatch as a function of the R_L mismatch.

Considering the inductance mismatch only, the maximum current difference can be found as

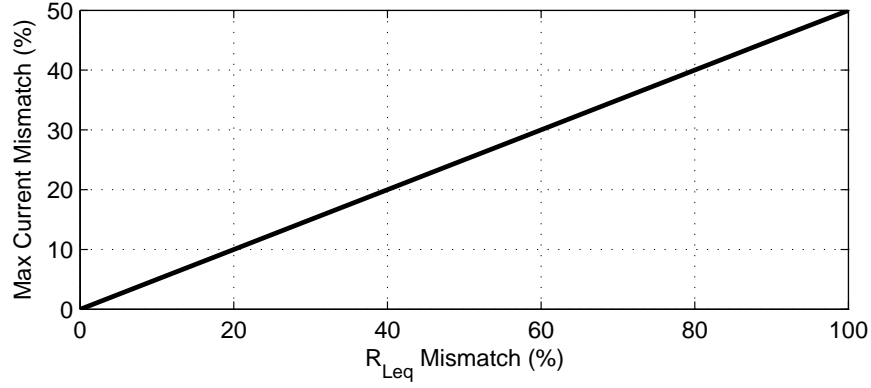


Figure 6.9: Maximum current mismatch using passive power sharing in two-phase boost PFC rectifier in CCM.

$$\mathbf{max} [\Delta i_L] \approx \frac{V_M}{2R_e} \cdot (\tau_L \omega_L) \cdot \frac{\Delta L}{L}, \quad (6.6)$$

where L is the nominal inductance (mean value of all the inductance) and τ_L is the nominal inductor time constant. Under an assumption that the inductor time constant τ_L is much shorter than one half of the line period T_L , the maximum current mismatch due to inductor mismatch Eq. 6.6 is much smaller than the current mismatch due to R_L mismatch, as Eq. 6.5. This conclusion is in contrast to the case when PFC rectifiers operate in DCM or in transition mode (CCM/DCM boundary) [68,69], when the current mismatch is caused mainly by the inductor value mismatch. Even in the case when the modules are perfectly matched, a current mismatch occurs in PFC rectifiers with passive power sharing due to phase-shifted control signals in combination with time-varying input voltage. By noting that the large-signal models averaged over a switching period (Fig. 6.7(b)) are linear, an s-domain approach based on the closed-loop model shown in Fig. 6.10 can be applied to examine this effect. The phase shift between the phases is modeled by a transfer function $G_d(s)$. The total inductor current i_L is well regulated by the current controller G_c to track the reference current ($i_{ref} = v_g/R_e$).

From the model in Fig. 6.10, the current mismatch can be found as

$$\Delta i_L(s) = \frac{v_g(s)}{R_e} \cdot \left[\frac{(G_d(s) - 1) \cdot (2G_{ig}(s) \cdot R_e - 1)}{\frac{1}{G_{id}(s) \cdot G_c(s)} + (1 + G_d(s))} \right], \quad (6.7)$$

From Eq. 6.7, it can be observed that the current mismatch is due to the phase shift ($G_d(s) \neq 1$), and the time-varying input voltage $v_g(s)$. Assuming a well-regulated input current, a first-order approximation for the delay transfer function $G_d(s)$, and a sinusoidal ac input voltage at 60 Hz, the maximum current mismatch is shown in Fig. 6.11 as a function of R_L/R_e for several values of the input voltage $V_{ac,rms}$, and inductance L . For heavy loads with dominant conduction loss, the current mismatch due to phase shift is relatively small. A more detail analysis of the current mismatch in passive power sharing is shown in Appendix B.

6.4 Over Current Protection

Although passive power sharing minimizes the conduction losses, as described in Sec. 6.3.1, the resulting current mismatch discussed in Sec. 6.3.2 may result in additional current stresses. Therefore, it is of interest to consider ways to provide per-module over-current protection without compromising the current-sensing simplicity and modularity of the passive power sharing approach. An over-current detection circuit proposed in this chapter is based on monitoring the charge-up time for the switching node capacitance (C_x) as an indication of the peak inductor current. Upon transistor turned-off interval, it takes time to charge C_x and lift switching node voltage v_{ds} up to the output voltage after the diode turns on. For a given v_g and C_x , the total required charge Q_c supplied by the inductor to charge C_x from 0 to v_g is a fixed value. The charge up time t_c is therefore inversely proportional to the inductor peak current $i_{L,peak}$, as

$$i_{L,peak} \cdot t_c = Q_c = \int_0^{v_g} C_x(v_{ds}) dv_{ds}. \quad (6.8)$$

As shown in Fig. 6.4, the DCM detection comparators are included to detect polarity change of the voltage across the inductor [79]. The same comparators can be used to determine the time when v_{ds} reaches v_g after the boost transistor is turned off, as shown in Fig. 6.12.

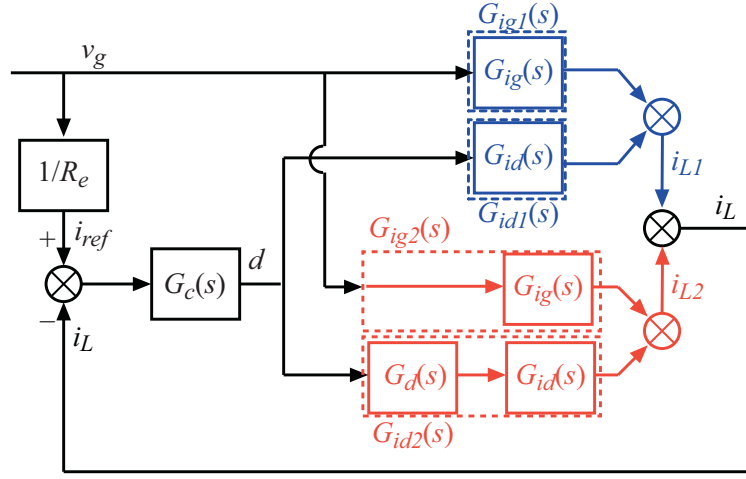


Figure 6.10: Two-phase interleaved PFC rectifier model, including phase shift modeled by $G_d(s)$.

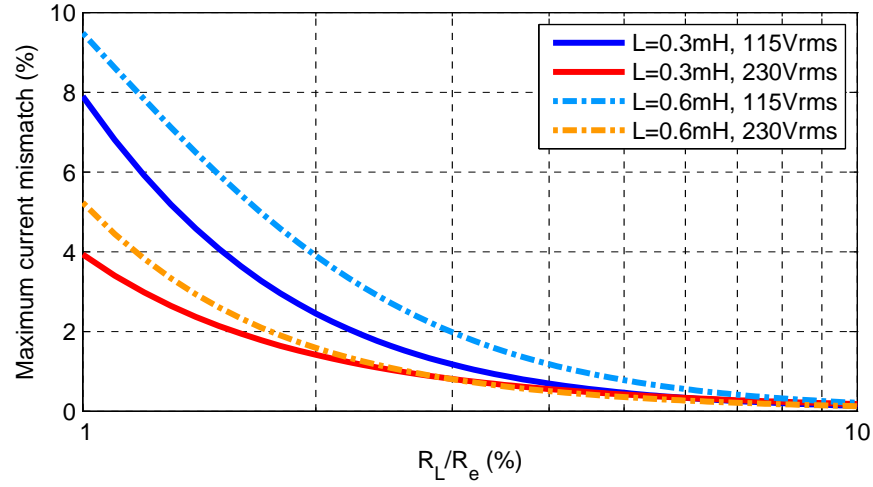


Figure 6.11: Maximum current mismatch using passive power sharing in the two-phase interleaved boost PFC rectifier in CCM. (600W, $f_s = 100\text{kHz}$, $f_L = 60\text{Hz}$).

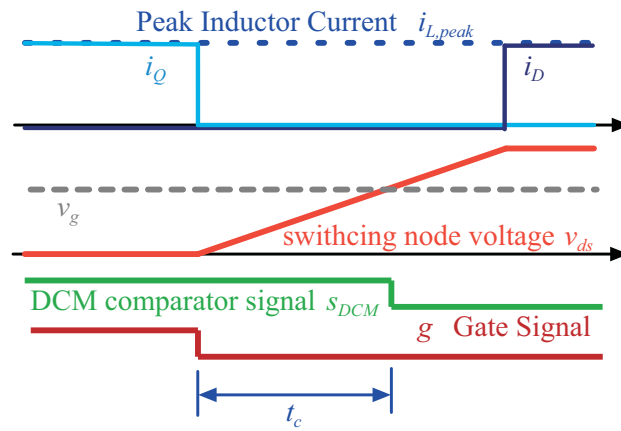


Figure 6.12: Waveforms during transistor turn-off interval.

The digital controller simply counts the time interval t_d between the gate signal g high-to-low transition and the corresponding transition in the DCM comparator signal S_{DCM} . It should be noted that t_d is a sum of the switching node charge-up time (t_c), gate drive delay ($t_{d,GD}$), and the comparator delay ($t_{d,COMP}$). The last two terms are highly dependent on the component selections and their variations, so a calibration is required in a practical implementation of the proposed over-current protection. Fig. 6.13 shows examples of v_{ds} waveforms for different inductor peak currents.

Most of t_d is when v_{ds} is low, which is due to the larger transistor drain to source capacitance at low v_{ds} . When v_{ds} is high, the charging-up slope is much steeper. The peak current occurs around the peak line voltage $v_g = V_M$, which corresponds to a lower capacitance as v_{ds} reaches v_g . Therefore, t_d increases only slightly with increasing input voltage, which means that the calibration can be performed at just one voltage. Time resolution of the digital controller system clock (10 ns in the experimental prototype) is too low for precise current detection. In order to measure t_d more precisely, a delay line based timer has been constructed as shown in Fig. 6.14, improving the timing resolution to about 2 ns.

Experimental results showing t_d as a function of $i_{L,peak}$ at $v_g = 100$ V are shown in Fig. 6.15. This result can be used to calibrate the proposed over-current protection function.

6.5 Phase Interleaving and Phase Shedding

In order to improve overall efficiency, phase shedding approaches have been developed for multi-phase interleaved PFC rectifiers [67, 77]. The main idea of phase shedding is to reduce the switching loss when PFC rectifier is processing less power. Most phase shedding PFC rectifiers reduce the number of active phases based on the power command (u), which makes the number of active phases be constant over the line period. Programmability of a digital controller makes the required scaling of the power command and the current loop gain adjustment easy. In addition to phase shedding, since the power processed by the PFC rectifier changes within a line period, approaches based on varying the switching frequency within a line period have been proposed in

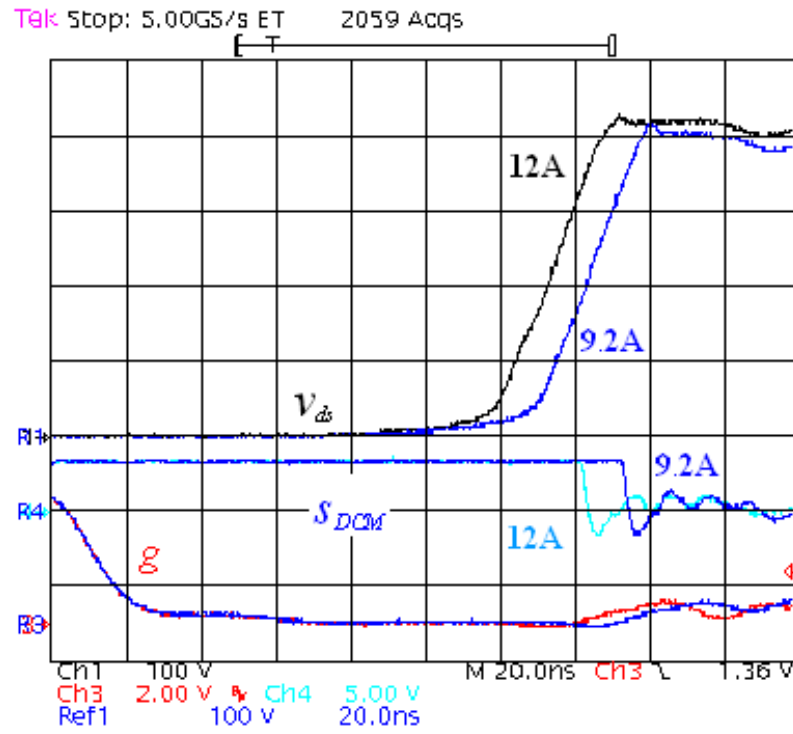


Figure 6.13: Experimental waveforms during transistor turn-off interval.

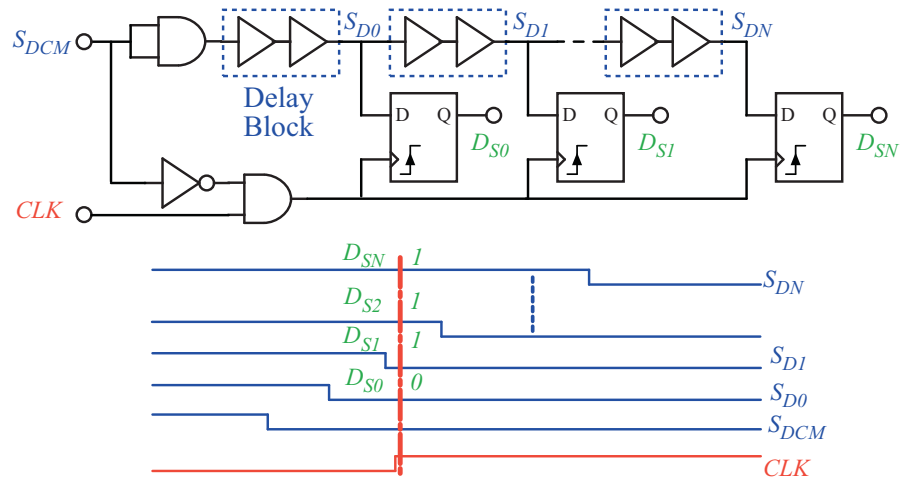


Figure 6.14: Delay line timer for improved resolution in measuring time interval t_d .

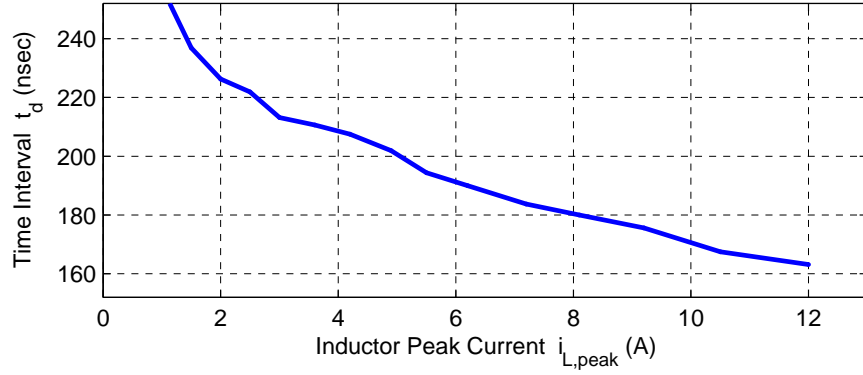


Figure 6.15: Time interval (t_d) as a function of the inductor peak current ($i_{L,peak}$) ($v_g = 100$ V, $Q(\text{STP21NM60N})$, $D(\text{FFPF04S60STU})$).

Chapter 3 and Chapter 4. For high efficiency over wide load range, the passive power sharing and adaptive approaches are combined together. In this section, issues related to light load efficiency improvement are discussed in more detail.

6.5.1 Phase Shifting with Adaptive Frequency Operation

The adaptive frequency approach changes the operating frequency to reduce switching loss at light loads. A constant time shift between the phases would result in additional current ripple. The approach implemented in the experimental prototype is based on a digital pulse-width modulator (DPWM) in a master phase operating as described in Chapter 3, while DPWM's in the slave phases replicate the master phase turn-on/turn-off intervals with an adaptive phase shift. The slave phases adjust turn-off time to achieve the required phase shift. The operation is illustrated by the waveforms in CCM and in DCM shown in Fig. 6.16 and Fig. 6.17, respectively.

6.5.2 Current Sensing

As shown in Fig. 6.4, the current analog-to-digital converter (ADC) samples the total inductor current in the middle of the transistor conduction interval. In CCM, with an even phase shift, the sensed current represents the total average current, as the two-phase example shows in Fig. 6.18. With an uneven phase shift, there would be an offset between the average inductor current

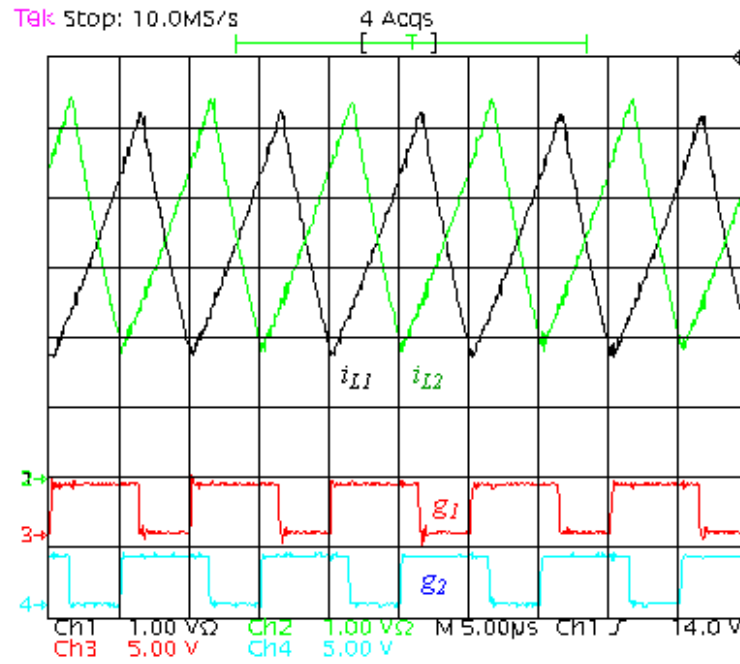


Figure 6.16: Experimental interleaved boost PFC converter waveforms in CCM, gate drive signals (g_1 , g_2) and inductor currents (i_{L1} , i_{L2}), adaptive frequency CCM/DCM current control ($f_{s,max} = 100$ kHz).

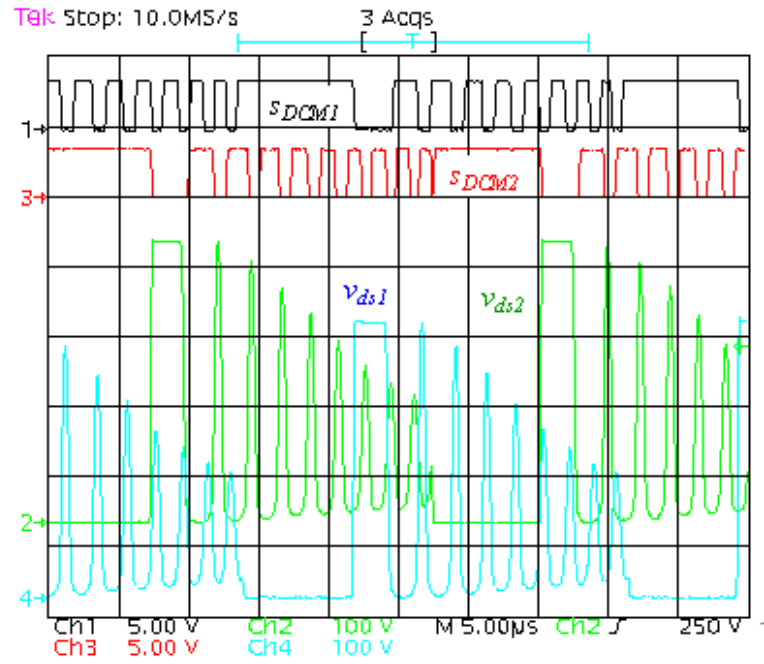


Figure 6.17: Experimental interleaved boost PFC converter waveforms in DCM, comparator signals (s_{DCM1} , s_{DCM2}) and transistor drain voltages (v_{ds1} , v_{ds2}), adaptive frequency CCM/DCM current control ($f_{s,max} = 100$ kHz).

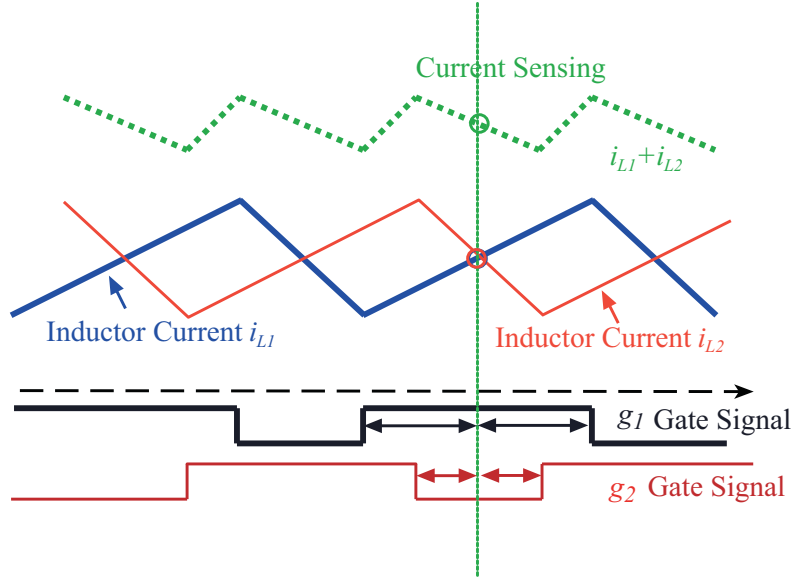


Figure 6.18: CCM current sense in passive power sharing approach (two-phase interleaved example).

and the sensed current, which would increase the current harmonic distortion.

In DCM, the current sensing correction factor, which is presented in Chapter 3, cannot be applied directly in the multi-phase configuration. In deep DCM, the sensed current may only represent part of the inductor current as shown in the example of Fig. 6.19. With an uneven phase shift in DCM, even larger current sensing errors can be expected.

However, it should be noted that the effects of the current sensing correction and the current sensing error in DCM are in the same direction, which means that the overall error between the real average current and the sensed current can be relatively small. Furthermore, most current distortion happens in deep DCM around zero-crossing of the line voltage, so that the overall effect on the input current distortion is small. Finally, as noted above, phase shedding reduces the number of active phases at light loads, and digital controller can make phase shedding be smooth, as illustrated in Fig. 6.20. Once the system operates with a single active phase, the DCM current correction described in Chapter 3 applies, and the light-load current harmonic distortion is reduced.

A final comment relates to application of the adaptive switching, which adjusts the switching period slightly to achieve switching at the lowest v_{ds} in DCM. In the multi-phase configuration, if

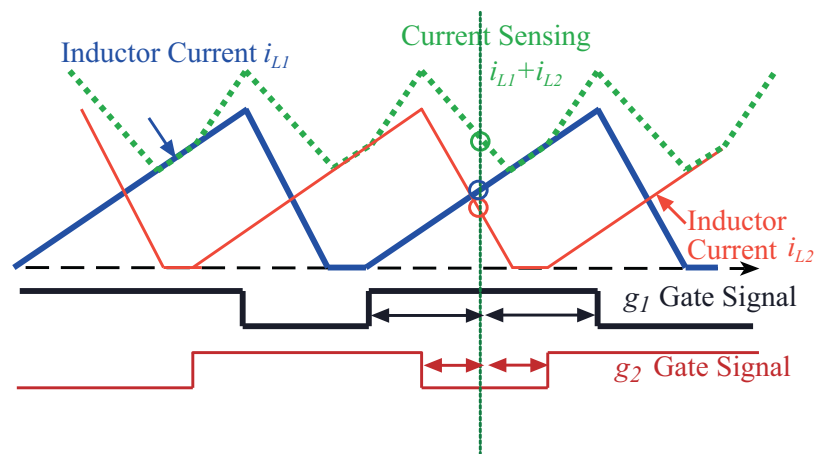


Figure 6.19: DCM current sense in passive power sharing approach (two-phase interleaved example).

all DPWM's are performing adaptive switching, the phase shift between the phases can be slightly off. Similar phenomena happen in transition mode interleaved PFC rectifiers, which have been addressed and discussed in [68, 69]. A phase lock loop (PLL) approach may not apply because of the discrete nature of the timing related to an integer number of DCM oscillation periods, resulting in sudden jumps in the switching periods. Fig. 6.21 shows how current sensing can be highly dependent on the discontinuous conduction period (T_{dcm}) in the previous switching period. This effect may cause some oscillations in the current loop, and a slight increase in input current distortion.

6.6 Results and Discussion

A 600W two-phase boost PFC rectifier ($f_s = 100$ kHz, $L_1 = L_2 = 320$ μ H, $C = 440$ μ F) has been built with a field programmable gate array (FPGA) platform implementing the digital controller. The experimental prototype is shown in Fig. 6.22.

For heavy load operation, the controller operates at constant frequency with two active phases interleaved and evenly phase-shifted by 180 degrees. The operating waveforms are shown in Fig. 6.23.

For moderate loads, two active phases operate in both CCM and DCM over a line period. The controller starts to reduce the switching frequency (Fig. 6.24) following the adaptive frequency approach. Because the DCM current sensing error discussed in Sec. 6.5.2 cannot be fully corrected, some additional current distortion can be observed. When the controller drops one phase, the remaining active phase operates in CCM as shown in Fig. 6.25.

Once phase shedding results in a single active phase, both adaptive switching and adaptive frequency are activated with DCM current correction as described in Chapter 3 and illustrated by the waveforms in Fig. 6.26. Compared to the two-phase constant frequency interleaved case (Fig. 6.27), the current distortion is reduced.

Efficiency improvements are illustrated in Fig. 6.28. The adaptive switching and the adaptive frequency approaches reduce switching losses at light loads, while phase shedding further improves

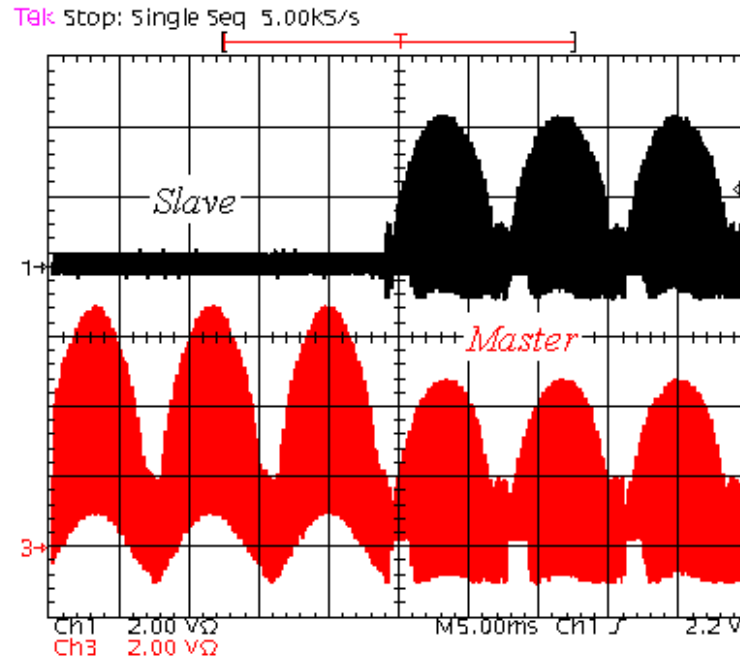


Figure 6.20: Experimental inductor current waveforms in master and slave phases (two-phase interleaved example) (≈ 300 W).

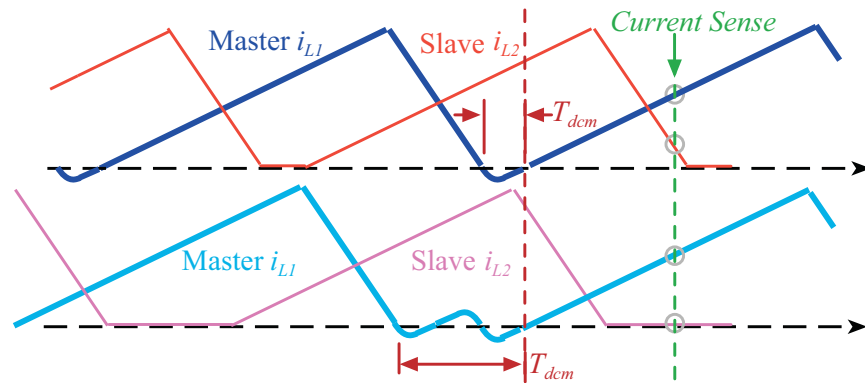


Figure 6.21: DCM current sense in passive power sharing approach (two-phase interleaved example) (Master - adaptive switching DPWM; Slave - follower DPWM).

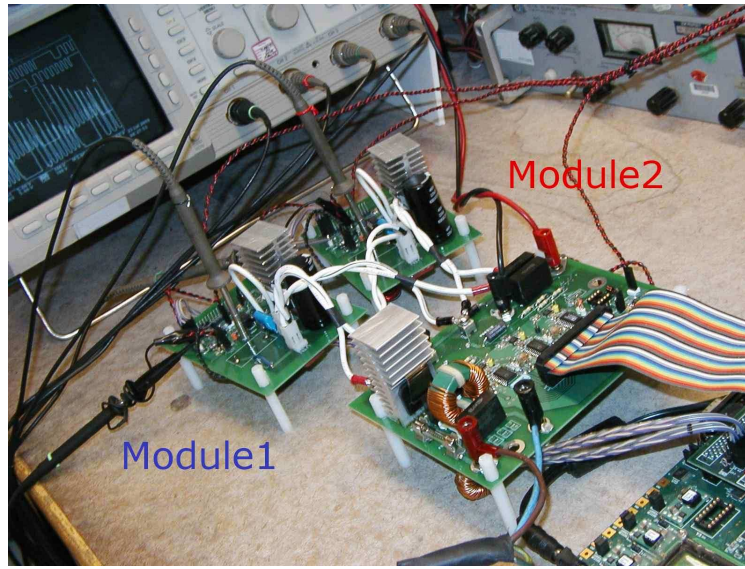


Figure 6.22: Experimental setup for 600W digitally controlled two-phase boost PFC rectifier.

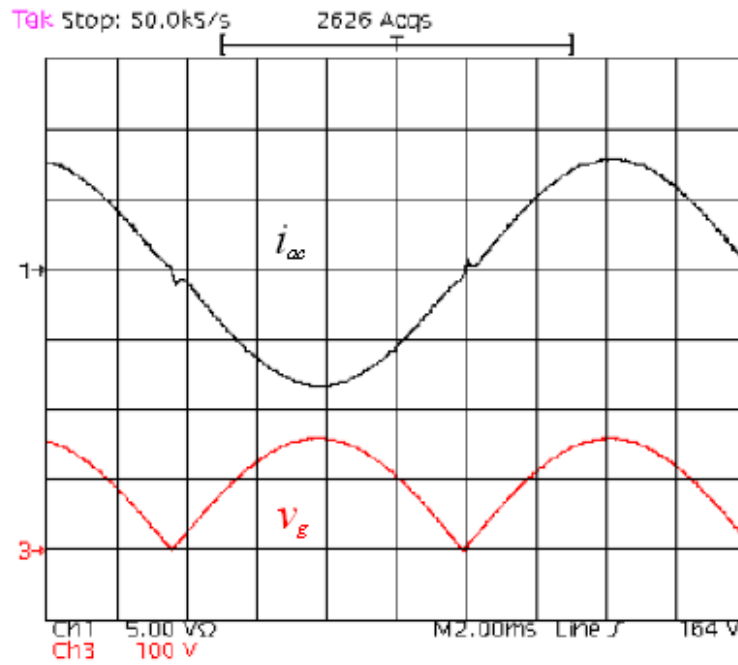


Figure 6.23: Experimental boost PFC converter waveforms, rectified line voltage v_g and line current i_{ac} , adaptive frequency approach ($f_{s,max} = 100$ kHz; 600 W; two active phases interleaved).

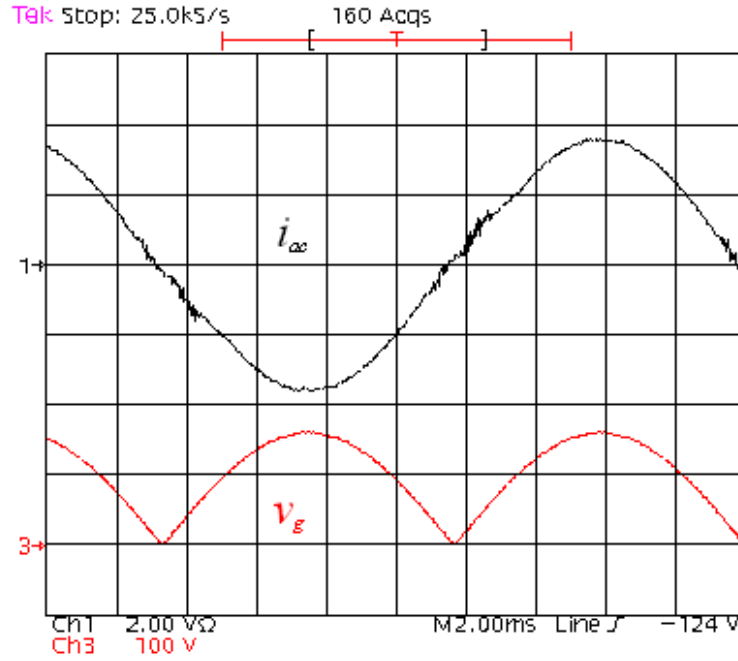


Figure 6.24: Experimental boost PFC converter waveforms, rectified line voltage v_g and line current i_{ac} , adaptive frequency approach ($f_{s,max} = 100$ kHz; 270 W; two active phases interleaved).

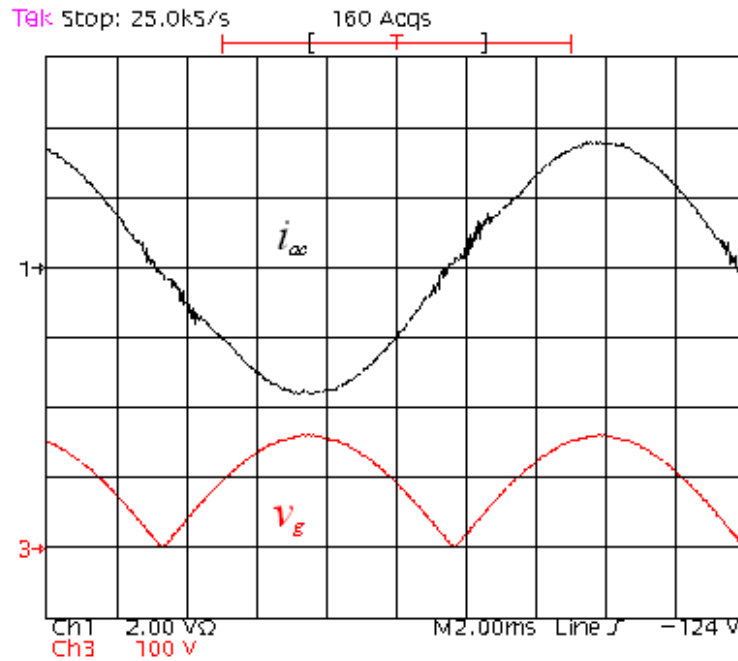


Figure 6.25: Experimental boost PFC converter waveforms, rectified line voltage v_g and line current i_{ac} , adaptive frequency approach ($f_{s,max} = 100$ kHz; $f_{s,min} = 40$ kHz; 270 W; single active phase).

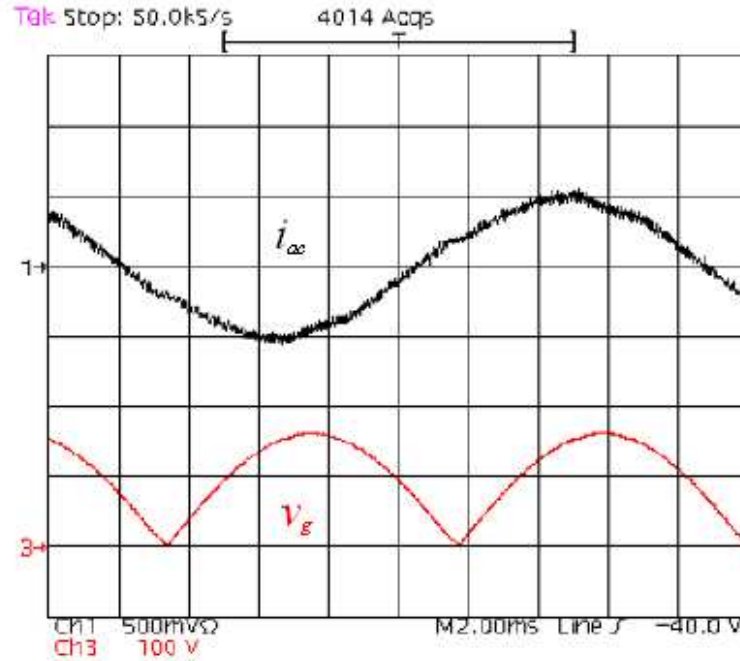


Figure 6.26: Experimental boost PFC converter waveforms, rectified line voltage v_g and line current i_{ac} , adaptive frequency approach ($f_{s,max} = 100$ kHz; $f_{s,min} = 40$ kHz; 30 W; single active phase).

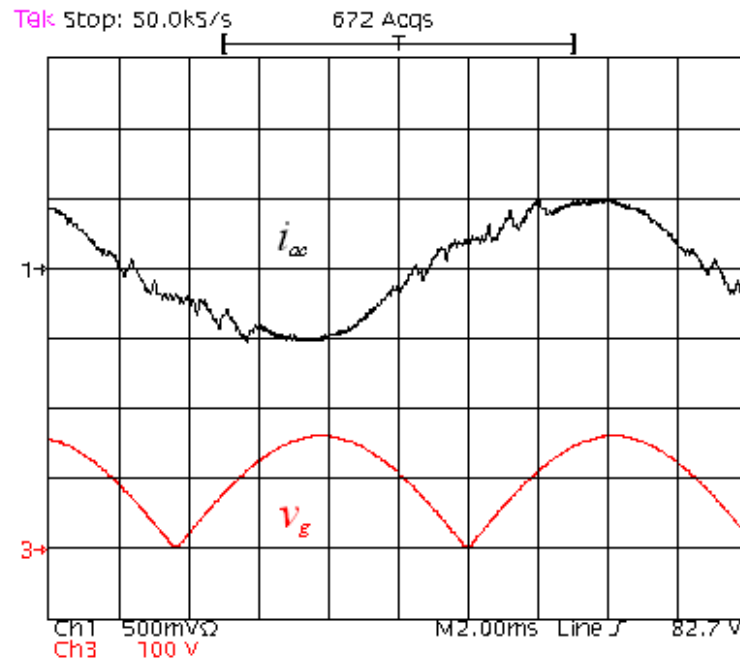


Figure 6.27: Experimental boost PFC converter waveforms, rectified line voltage v_g and line current i_{ac} , predictive current approach ($f_s = 100$ kHz; 30 W; two active phases interleaved).

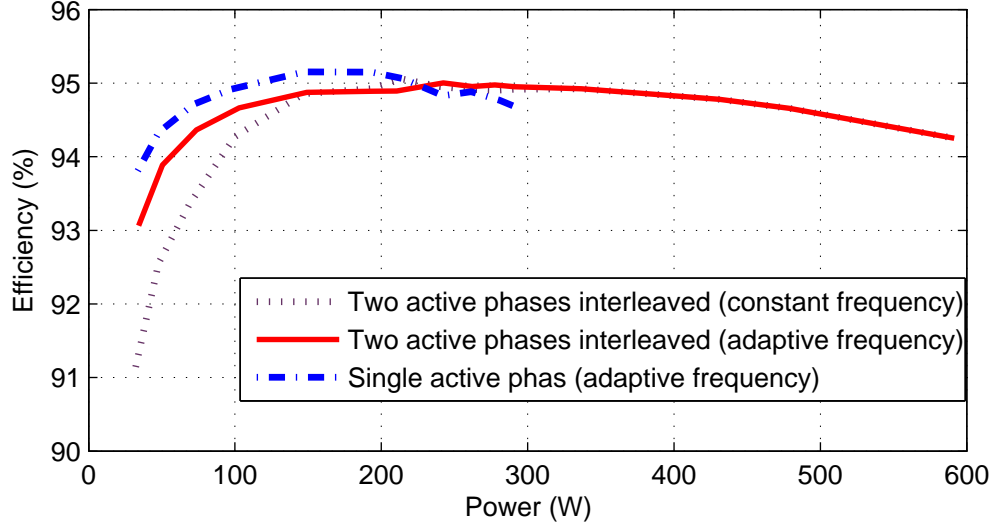


Figure 6.28: Experimental efficiency comparison ($v_{g-rms} = 115$ V; $f_{s,max} = 100$ kHz; $f_{s,min} = 40$ kHz).

the light load efficiency. The experimental efficiency results indicate that phase shedding should be activated when the power drops below 270 W, leaving one phase active. At very light load (30 W), efficiency is improved by about 3% compared to the conventional two-phase system operating at constant switching frequency.

Chapter 7

Conclusions

Low current harmonic distortion, low cost and high efficiency are always the targets for power factor correction (PFC) rectifiers. Today, driven by economic reasons and concerns about the environment, maintaining high efficiency and good power factor over wide load range has become the main demand in PFC rectifiers. Instead of using high performance components to reduce loss or adding many extra components to achieve soft switching with complicated controllers, this thesis proposes simple low cost digital control techniques to maintain high efficiency and low current harmonic distortion over a wide range of loads in single-phase boost PFC rectifiers.

The next section summarizes the original contributions of this thesis followed by future related research directions.

7.1 Summary of Contributions

(1) **Development of current sensing correction factor using measured discontinuous conduction period:**

Generally, digital boost PFC controllers sense inductor current at the middle of the transistor or diode conduction period to represent average inductor current in continuous conduction mode (CCM). This is no longer valid in discontinuous conduction mode (DCM). With the estimated current sensing correction factor, the single controller can operate in both CCM and DCM in boost PFC rectifiers [48]. Instead of applying the estimated current sensing correction factor, a measurement based current sensing correction factor is intro-

duced in Chapter 3, which takes advantage of a DCM comparator and a counter in the digital controller to measure the discontinuous conduction period. Using the measured discontinuous conduction period, the current sensing correction factor can be easily calculated and applied to boost PFC rectifiers [79, 80].

(2) Development of adaptive switching CCM/DCM current control:

Adaptive switching CCM/DCM current control applies the current sensing correction factor and the adaptive switching technique in DCM to a predictive current control law [79, 80]. The adaptive switching approach runs the same as the predictive current control in CCM and adjusts transistor turn-on timing to achieve low voltage switching in DCM (Chapter 3). Using the information from the DCM comparator, which senses voltage polarity change across the inductor, adaptive switching approach turns the transistor on at the lowest drain voltage in DCM saving part of the discharge energy loss due to switching node capacitance. In addition, it also reduces the current harmonic distortion due to the DCM oscillation described in Chapter 2.

(3) Development of adaptive frequency CCM/DCM current control:

Adaptive frequency CCM/DCM current control is based on adaptive switching CCM/DCM control with additional switching frequency adaptation in DCM [79, 80]. The adaptive frequency technique shapes the inductor current by changing the switching period instead of changing the duty ratio in DCM (Chapter 4). Since the power processed across the line period changes a lot in PFC rectifiers, the adaptive frequency technique adjusts the switching frequency over the line period. This further reduces switching loss at light load and improves current shaping in DCM. A minimum switching frequency setup prevents audible noise but introduces some current harmonic distortion at very light load operation.

(4) Development of current error estimation for boost PFC rectifiers in both CCM and DCM:

Current error estimation technique estimates the current error in both CCM and DCM

using a slow digital to analog converter (DAC) and a single inductor current comparator (Chapter 5). The existing analog to digital converter (ADC) for current sensing requires high speed and high resolution, and it could be affected by the switching noise since boost PFC rectifiers have the duty ratio from almost 0% to 100%. Current error estimation trades the time resolution for the ADC resolution and removes the needs for precise current sampling. The combination of current error estimation and predictive current controller form a current controller independent of inductor value, which reduces design effort and improves robustness of the current loop. The current error estimation can also be applied in combination with adaptive CCM/DCM controller to achieve high efficiency over wide load range.

(5) **Analysis of passive power sharing in interleaved boost PFC rectifier:**

Passive power sharing can be adopted in interleaved boost PFC rectifiers to increase system power modularity [81]. It can reduce total inductor current ripple without extra current sensing circuits. Chapter 6 examines the tradeoff between reduction of the conduction loss and inductor current mismatch when the simple passive power sharing technique is applied.

(6) **Development of over current protection technique for passive power sharing:**

Based on the possible current mismatch in passive power sharing, a new over current protection circuit is introduced in Chapter 6. The circuit measures the switching node charge-up time as an indication of inductor peak current [81]. Based on the gate drive signal and the DCM comparator signal, switching node charge up time can be counted by the delay line enhanced digital counter.

7.2 Related Future Research Directions

This thesis addressed operation and digital control of boost PFC rectifiers operating over wide load range. Some of the potential research directions related to this work include:

(1) **Current error estimation in interleaved boost PFC rectifiers:**

The proposed current error estimation could be implemented in interleaved boost PFC rectifiers. For interleaved boost rectifiers, the current control algorithm using current error estimation is no longer independent of inductor values. This requires more investigation related to the inductor mismatch.

(2) Resolution of current error estimation:

Current error estimation trades time resolution for the ADC resolution. However, most digital signal processors (DSP) are running at lower frequency clocks. Using multiple comparators for current error estimation could be applied to relieve time resolution requirements.

Appendix A

DCM Switch

In order to reduce discontinuous conduction mode (DCM) oscillation in boost power factor correction (PFC) rectifiers, the DCM switch approach is proposed in Chapter 3. The main idea is to store DCM oscillation energy from the switching node capacitance to the inductor. A secondary winding is added on the inductor with a switch (Q_{DCM}) across the secondary winding, as shown in Fig. A.1. During discontinuous conduction interval (T_{dcm}), when switching node voltage rings to the rectified input voltage (v_g), the proposed controller sets the gate signal of the DCM switch (g_{DCM}) high to make DCM oscillation energy stored in the magnetic inductance (L_M) and to circulate current through Q_{DCM} . In order to switch Q_{DCM} on at the correct time, a DCM comparator is added to measure inductor voltage (v_L) polarity. DCM comparator signal (s_{DCM}) also helps to detect the CCM/DCM boundary and to measure T_{dcm} , which can reduce current harmonic distortion in DCM (Fig. A.2).

Detailed design of the dead-time between the DCM switch (Q_{DCM}) and the boost transistor (Q) is shown in Sec. A.1. It is followed by a discussion of DCM switch implementation in Sec. A.2. The final section shows the experimental results and discussion.

A.1 Dead-Time Analysis

When the boost transistor starts to conduct, energy stored in the switching node capacitance (C_x) is discharged immediately through the transistor (Fig. A.3). Adding some dead-time (T_D) between boost gate drive signal (g) and DCM switch gate signal (g_{DCM}) recycles some energy

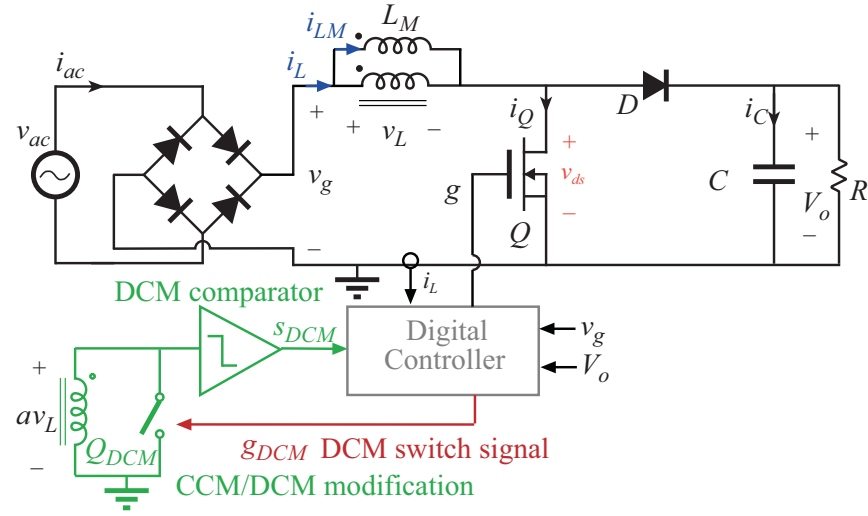


Figure A.1: Block diagram of a boost PFC rectifier using DCM switch.

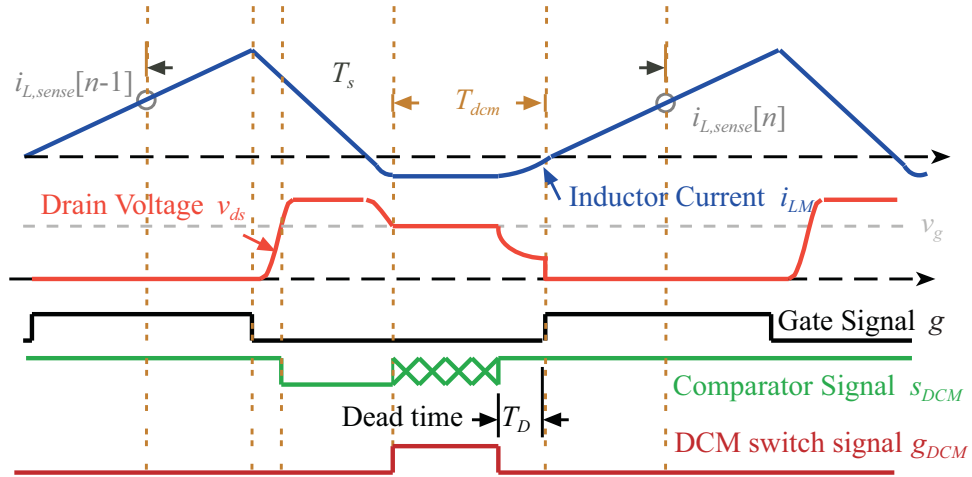


Figure A.2: Operation waveforms illustrating DCM switch approach.

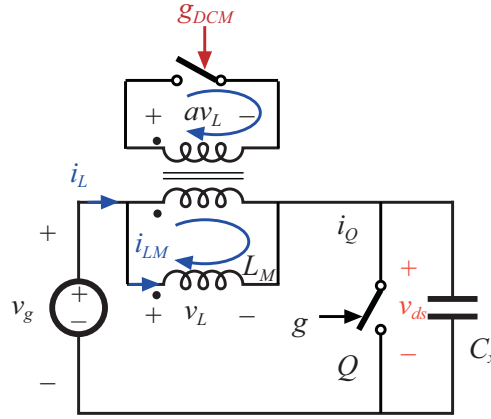


Figure A.3: Circuits of DCM switch.

stored in C_x , as illustrated in Fig. A.2.

Adding some dead-time helps to move some energy from C_x to the input capacitor. During the dead-time, there is no circulation current flowing through the DCM switch; however, there is still energy stored in the magnetizing inductance (L_M). Before the boost transistor conducts, energy stored in C_x is transferred to L_M , which reduces the switching node voltage v_{ds} . Applying proper dead-time enables the boost power transistor to turn on at low voltage. The dead-time can be analyzed by using state plane analysis.

In state plane analysis, as shown in Fig. A.4, the ideal dead-time is to follow the dash line, which turns the boost main switch on at the lowest switching node voltage (v_{ds}). By finding a constant equivalent capacitance at the switching node, constant dead-time can be applied to achieve low voltage turn-on.

A.2 Switch Implementation

From the circuit implementation point of view, the DCM switch has to be able to block both positive and negative voltages and allow the current to flow in one direction. Two topologies can functionally work for the DCM switch (Fig. A.5): one is using back-to-back n-channel transistors with their sources tied together; the other is using a transistor in series with a diode.

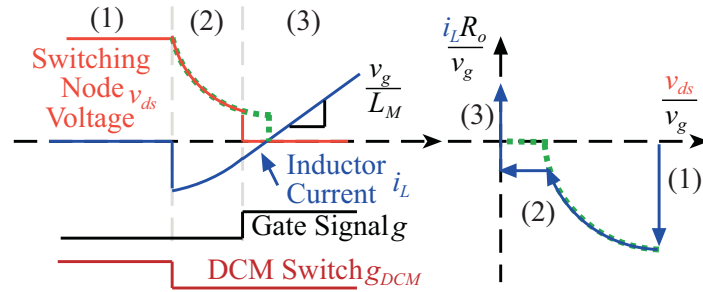


Figure A.4: Waveforms and state plane for dead-time analysis of DCM switch.

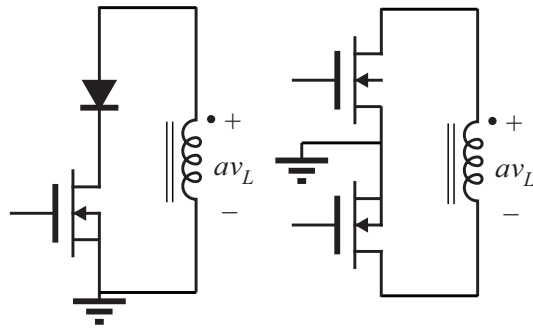


Figure A.5: Topologies of DCM switch implementation.

In the diode approach, by assuming the voltage drop due to the transistor on-resistance is smaller than the diode voltage drop (V_D), inductor current equation can be simplified as

$$L_M \cdot \frac{di_{LM}}{dt} = \frac{1}{a} \cdot V_D, \quad (\text{A.1})$$

where a is the turns-ratio between secondary winding and primary winding of the inductor.

With the discontinuous conduction interval (T_{dcm}) passing, the circulation current in the magnetic inductor decreases as

$$L_M(T_{dcm}) = i_{LM}(0) - \frac{V_D \cdot T_{dcm}}{a^2 \cdot L_M}. \quad (\text{A.2})$$

Applying similar analysis on a back-to-back transistors case, it becomes a simple LR damping, where the damping resistance is twice the on-resistance (R_{on}) of the transistors. The inductor current equation is

$$L_M \cdot \frac{di_{LM}}{dt} = i_{LM} \cdot \frac{2R_{on}}{a^2}. \quad (\text{A.3})$$

The inductor current at the end of the switching can be expressed as

$$L_M(T_{dcm}) = i_{LM}(0) - e^{\frac{-2R_{on} \cdot T_{dcm}}{a^2 \cdot L_M}}. \quad (\text{A.4})$$

By taking the derivative of Eq. A.3 and Eq. A.4 with respect to T_{dcm} , it can be observed that the slope of current reduction is related to the device parameters and the inductor initial current, $i_{LM}(0)$. For the low $i_{LM}(0)$ case, diode approach always makes more damping compared to the back-to-back transistors approach. The turns-ratio (a) of the inductor is related to the damping and the component selection. The lower the turns-ratio is, the higher the component voltage ratings are required, which may lead to higher on-resistance. The parasitic capacitance of the large devices is usually higher than that of the smaller devices. On the other hand, a higher turns-ratio makes the circulation current higher, which increases the effective damping. The selection of the turns-ratio

	Power	Efficiency	Power Factor	THD
CCM Predictive Current Control	100W	95.3%	0.991	9.3%
CCM/DCM Current Control with DCM Switch	100W	95.4%	0.999	2.3%
CCM Predictive Current Control	15W	90.1%	0.976	18.3%
CCM/DCM Current Control with DCM Switch	15W	91.4%	0.978	6.8%

Table A.1: Performance comparison of experimental CCM predictive current controller and predictive CCM/DCM current controller with DCM switch ($v_{ac,rms} = 110V$; $f_s = 80kHz$)(transistor: STP25NM60N; diode: CSD04060).

and the damping loss is a design tradeoff. Lower voltage rating components have lower cost and can be combined with the DCM comparator circuits easily. Hence, $a = 1/10$ ratio with back to back transistors (NDT3055) are selected for the DCM switch implementation.

A.3 DCM Switch Results and Discussion

First, experimental waveforms that illustrate the DCM switch operation are shown in Fig. A.6. The DCM switch dramatically reduces the DCM oscillation. Applying the proper dead-time between DCM switch turn off and boost switch turn on, the DCM switch can achieve low voltage turn-on, as shown in Fig. A.7.

The DCM switch starts to operate at medium to light load range when the boost power stage is operated in DCM for part of the line period. Experimental waveforms, ac line current i_{ac} and rectified line voltage v_g , are shown in Fig. A.8 and Fig. A.9, which illustrate the low current harmonic distortion in boost PFC rectifier achieved by using the DCM switch. However, due to the on-resistance damping and extra capacitance at the switching node, efficiency improvement with the DCM switch is relatively small. Results are summarized in Table A.1.

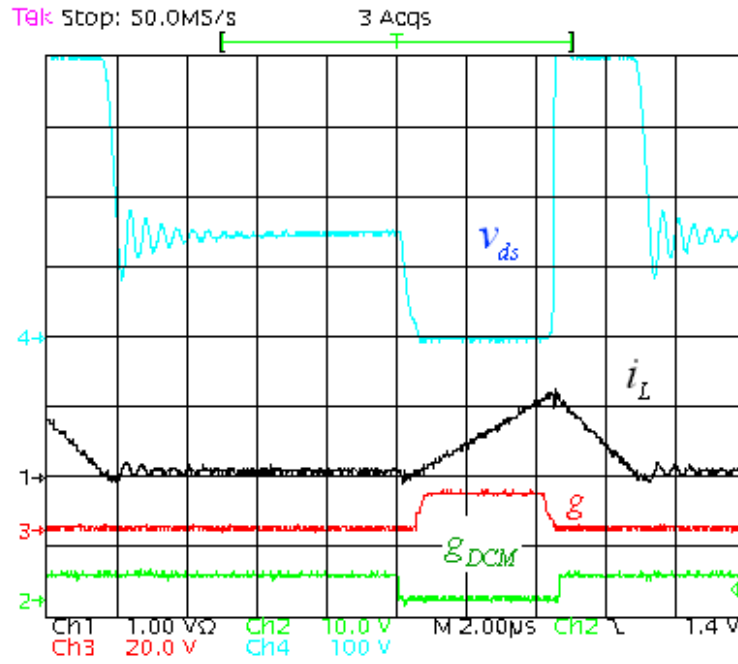


Figure A.6: Experimental waveforms of the DCM switch with dead-time, gate control signal (g), drive signal for DCM switch (g_{DCM}), transistor drain voltage (v_{ds}), and inductor current (i_L) ($f_s = 80$ kHz)..

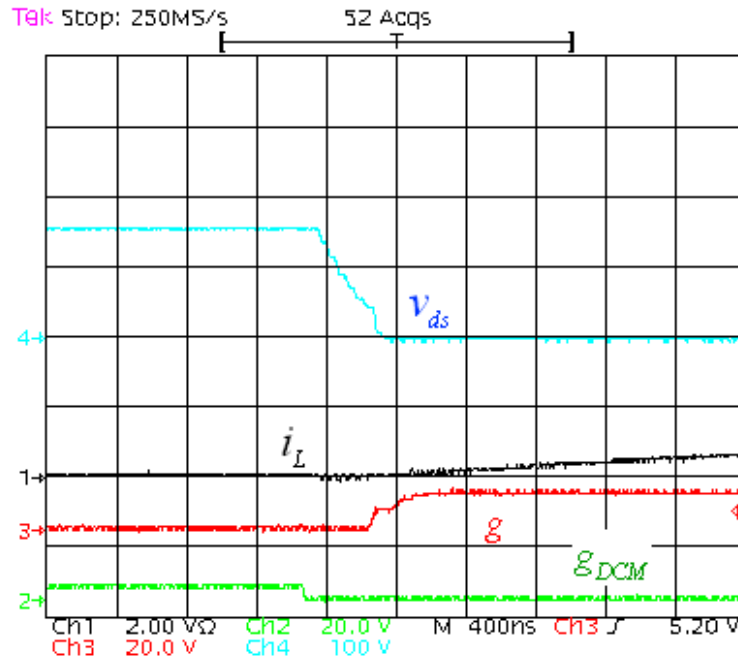


Figure A.7: Experimental waveforms of the DCM switch with dead-time, gate control signal (g), drive signal for DCM switch (g_{DCM}), transistor drain voltage (v_{ds}), and inductor current (i_L) ($f_s = 80 \text{ kHz}$) (zoom-in at transistor turn on interval).

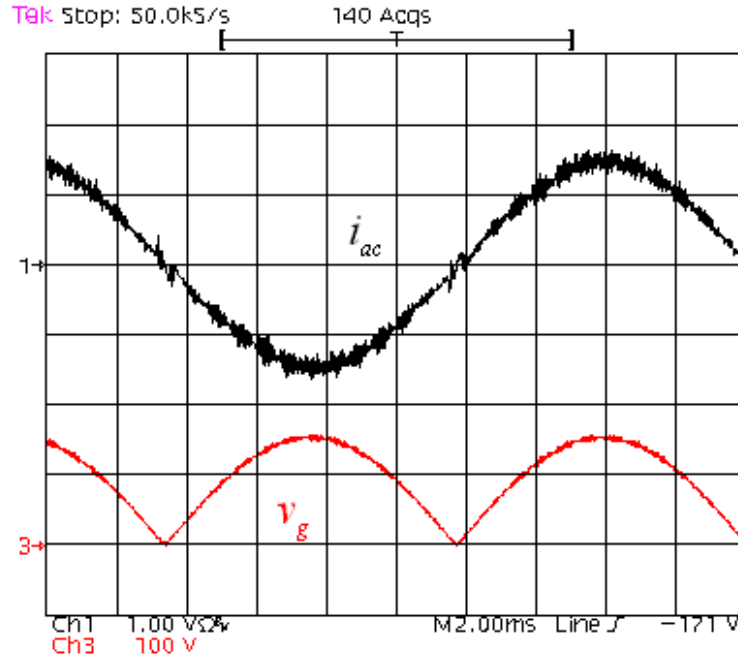


Figure A.8: Experimental boost PFC converter waveforms, rectified line voltage v_g and line current i_{ac} , with the DCM switch ($f_s = 80$ kHz; 100 W).

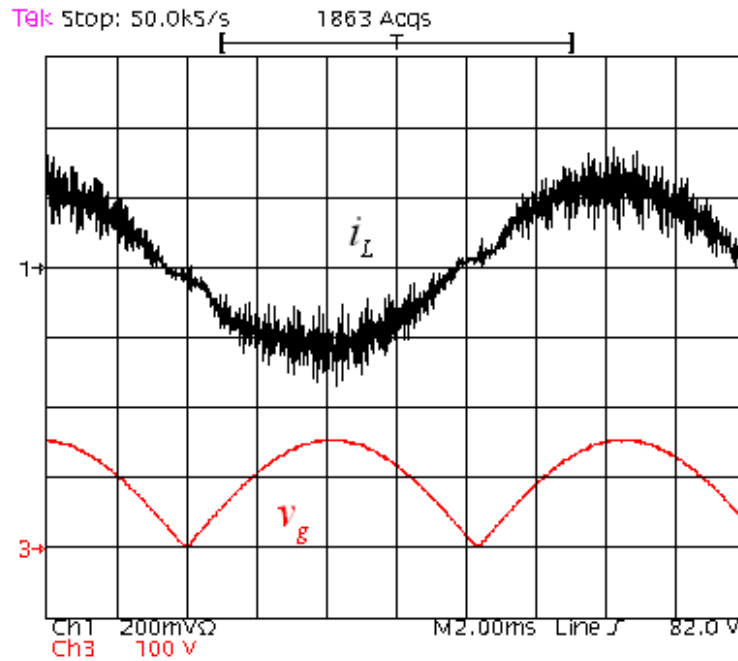


Figure A.9: Experimental boost PFC converter waveforms, rectified line voltage v_g and line current i_{ac} , with the DCM switch ($f_s = 80$ kHz; 15 W).

Appendix B

Passive Power Sharing Analysis

This appendix contains an analysis of the interleaved boost power factor correction (PFC) rectifier discussed in Chapter 6. The first section presents the efficiency analysis with active power sharing, or with passive power sharing when considering conduction losses only. Then, the second section discusses current mismatches in passive power sharing, including component mismatch effects and phase interleaving effects.

B.1 Efficiency in PFC rectifier with Active or with Passive Power Sharing

In boost PFC rectifiers, the conduction loss in the boost power stage can be modeled as shown in the averaged circuit model in Fig. B.1 [8]. The model contains losses due to inductor winding resistance (R_L), losses due to transistor turn-on resistance (R_{on}), and losses due to diode forward voltage drop (V_F) under the condition that rectified line voltage ($v_g(t)$) and duty cycle ($d(t)$) vary with time. Based on the model illustrated in Fig. B.1, system efficiency can be calculated. However, since duty ratio is coupled with R_{on} and V_F terms, analytical solution is complicated. To simplify the analysis, the conduction loss can be modeled as an equivalent resistor (R_{Leq}) in series with a lossless emulated resistance (R_e), which transfers power to the output, as shown in Fig. B.2 for the two-phase boost PFC rectifier example.

This section discusses the efficiency difference between active power sharing and passive power sharing in a two-phase interleaved boost PFC rectifier example, based on the model in Fig. B.2. To verify reduction of the conduction loss in passive power sharing, a numerical analysis will be

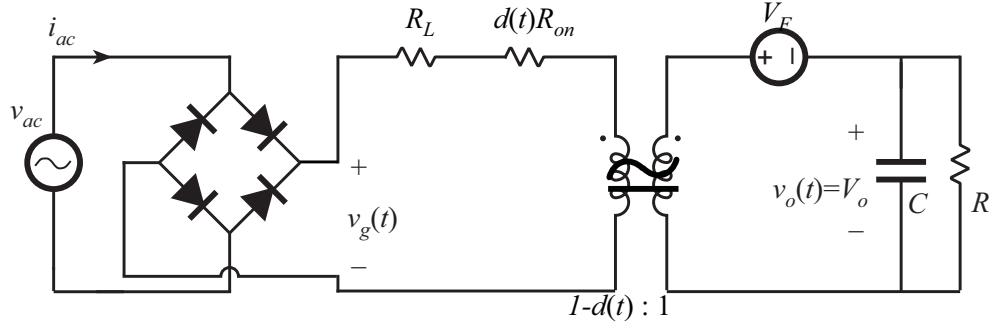


Figure B.1: A low frequency equivalent circuit for boost rectifier that models converter conduction losses.

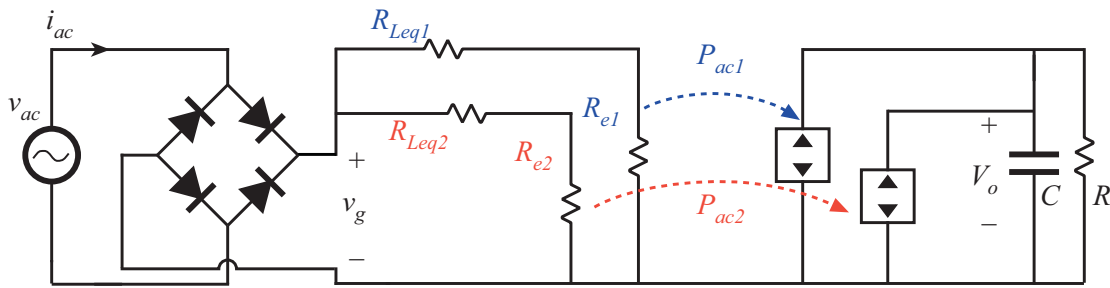


Figure B.2: Averaged equivalent circuit model of a two-phase boost PFC rectifier, including conduction loss equivalent resistance (R_{Leq1} , R_{Leq2}).

shown in the final part of this section.

B.1.1 Efficiency with Active Power Sharing

Active power sharing regulates the average inductor current ($\langle i_L \rangle_{T_s}$) at each phase to be the same and gives the required duty ratio ($d_i = 1 - d'_i$) for each phase, $i = 1, 2$. For investigating the current loop dynamics only, the output voltage can be regarded as a constant (V_o) as long as the output voltage variation is much smaller than the output voltage DC value. Inductor current dynamics, therefore, depends only on averaged rectified input voltage ($\langle v_g \rangle_{T_s}$), V_o and R_{Leq} . Based on the assumption, the averaged switch model of a two-phase boost PFC rectifier with active power sharing is shown in Fig. B.3.

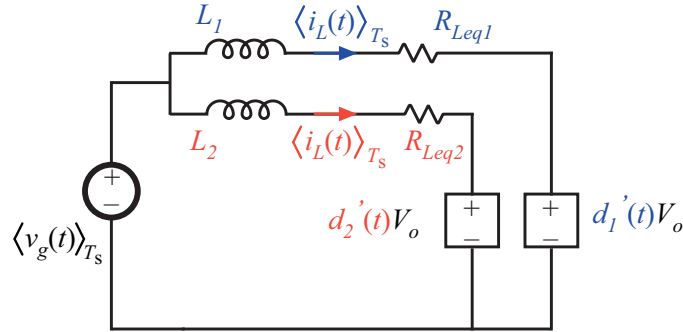


Figure B.3: Averaged switch model in boost PFC rectifier with active power sharing (two-phase example).

Here, $\langle v_g \rangle_{T_s}$ is rectified from the ac side input voltage, as

$$\langle v_g(t) \rangle_{T_s} = V_M \cdot |\sin(2\pi f_L t)|, \quad (\text{B.1})$$

where V_M is the peak line voltage and f_L is the line frequency. Ideally, active power sharing equalizes the current processed in each phase. Inductor currents in each phase are

$$\langle i_{L1}(t) \rangle_{T_s} = \langle i_{L2}(t) \rangle_{T_s} = \frac{V_M}{R_e} \cdot |\sin(2\pi f_L t)|. \quad (\text{B.2})$$

In active power sharing, the inductor currents are only decided by the current controller but not decided by the inductor value (L) or the conduction loss resistor (R_{Leq}). One important assumption is that time constant of the inductor ($\tau_L = L/R_L$) is much smaller than half of the line period (T_L). Hence,

$$\frac{\langle v_g(t) \rangle_{T_s}}{2R_e} \cdot R_{Leqi} \approx \langle v_g(t) \rangle_{T_s} - d'_i(t) \cdot V_o. \quad (\text{B.3})$$

Duty ratio in each phase can be calculated as

$$1 - d_i(t) = d'_i(t) = \frac{\langle v_g(t) \rangle_{T_s}}{V_o} \cdot \left(1 - \frac{R_{Leqi}}{2R_e} \right). \quad (\text{B.4})$$

The total average output current (I_o) can be written as the sum of the two diode average currents ($\langle i_{d1} \rangle_{T_s}$, $\langle i_{d2} \rangle_{T_s}$), as

$$\begin{aligned} I_o &= \frac{2}{T_L} \left[\int_0^{T_L/2} \left(\langle i_{d1}(t) \rangle_{T_s} + \langle i_{d2}(t) \rangle_{T_s} \right) dt \right] \\ &= \frac{V_M^2}{2R_e V_o} \left[\left(1 - \frac{R_{Leq1}}{2R_e} \right) + \left(1 - \frac{R_{Leq2}}{2R_e} \right) \right]. \end{aligned} \quad (\text{B.5})$$

Total input power (P_{in}) and output power (P_{out}) can be found as

$$P_{out} = V_o \cdot I_o = \frac{V_M^2}{4R_e} \left[\left(1 - \frac{R_{Leq1}}{2R_e} \right) + \left(1 - \frac{R_{Leq2}}{2R_e} \right) \right], \quad (\text{B.6})$$

$$P_{in} = \frac{V_M^2}{2R_e}. \quad (\text{B.7})$$

Let $R_{Leq,cm} = (R_{Leq1} + R_{Leq2})/2$ and $\Delta R_L = |R_{Leq1} - R_{Leq2}|$. Therefore, the efficiency in active power sharing is shown as

$$\eta_{active} = 1 - \frac{R_{Leq,cm}}{2R_e}. \quad (\text{B.8})$$

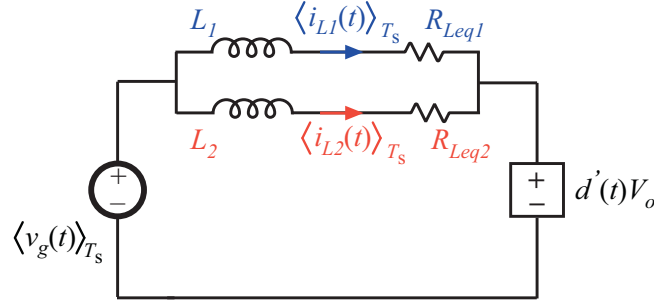


Figure B.4: Averaged switch model in boost PFC rectifier with passive power sharing (two-phase example).

B.1.2 Efficiency in Passive Power Sharing

Passive power sharing gives the same duty ratio for each phase, and allows the inductor currents to be as they are. The averaged switch model of the two-phase boost PFC rectifier using passive power sharing is shown in Fig. B.4.

Total inductor current ($\langle i_L \rangle_{T_s}$) is shaped by the current controller, which can be expressed as

$$\langle i_L(t) \rangle_{T_s} = \frac{\langle v_g(t) \rangle_{T_s}}{R_e} = \langle i_{L1}(t) \rangle_{T_s} + \langle i_{L2}(t) \rangle_{T_s}. \quad (\text{B.9})$$

From the average model in passive power sharing (Fig. B.4), the voltage across inductor (L) and the conduction loss resistor (R_{Leq}) in all the phases are the same. The voltages across the inductor are

$$\langle v_g(t) \rangle_{T_s} - d'(t) \cdot V_o = L_1 \frac{d \langle i_{L1}(t) \rangle_{T_s}}{dt} + \langle i_{L1}(t) \rangle_{T_s} \cdot R_{Leq1}, \quad (\text{B.10})$$

$$\langle v_g(t) \rangle_{T_s} - d'(t) \cdot V_o = L_2 \frac{d \langle i_{L2}(t) \rangle_{T_s}}{dt} + \langle i_{L2}(t) \rangle_{T_s} \cdot R_{Leq2}. \quad (\text{B.11})$$

Eliminating one of the variables from the previous two equations, the inductor current can be expressed as a first order ordinary differential equation, as

$$(L_1 + L_2) \frac{d\langle i_{L1}(t) \rangle_{T_s}}{dt} + \langle i_{L1}(t) \rangle_{T_s} \cdot (R_{Leq1} + R_{Leq2}) = \frac{L_2}{R_e} (2\pi f_L) V_M \cdot \cos(2\pi f_L t) + \frac{R_{Leq2}}{R_e} V_M \cdot \sin(2\pi f_L t) \quad (B.12)$$

With the initial condition at input voltage zero-crossing, $\langle i_{L1}(0) \rangle_{T_s} = \langle i_{L2}(0) \rangle_{T_s} = 0$, the average output current ($\langle i_o \rangle_{T_s}$) becomes

$$\begin{aligned} \langle i_o(t) \rangle_{T_s} = & \frac{A_1}{V_o} \frac{V_M}{R_e} \left[R_{L1} - L_1 \frac{(R_{Leq1} + R_{Leq2})}{(L_1 + L_2)} \right] \left[e^{-t \cdot \frac{(R_{Leq1} + R_{Leq2})}{(L_1 + L_2)}} \right] \left[\sin(2\pi f_L t) \right] \\ & - \frac{V_M}{R_e V_o} \left[B_1 L_1 \cdot 2\pi f_L + A_1 R_{Leq1} \right] \left[\sin(2\pi f_L) \cdot \cos(2\pi f_L t) \right] \\ & + \frac{V_M}{R_e V_o} \left[V_M + A_1 L_1 \cdot 2\pi f_L - B_1 R_{Leq1} \right] \left[\sin^2(2\pi f_L t) \right] \end{aligned} \quad (B.13)$$

where

$$A_1 = \frac{2\pi f_L V_M}{R_e} \frac{[(R_{Leq1} + R_{Leq2}) L_2 - (L_1 + L_2) R_{Leq2}]}{[(R_{Leq1} + R_{Leq2})^2 + (L_1 + L_2)^2 (2\pi f_L)^2]}, \quad (B.14)$$

$$B_1 = \frac{V_M}{R_e} \frac{[(R_{Leq1} + R_{Leq2}) R_{Leq2} + (L_1 + L_2) (2\pi f_L)^2 L_2]}{[(R_{Leq1} + R_{Leq2})^2 + (L_1 + L_2)^2 (2\pi f_L)^2]}. \quad (B.15)$$

The total input power and output power can be described as

$$P_{out} = V_o \cdot \int_0^{T_L/2} \langle i_o(t) \rangle_{T_s} dt, \quad (B.16)$$

$$P_{in} = \frac{V_M^2}{2R_e}. \quad (B.17)$$

Therefore, the efficiency with passive power sharing is

$$\begin{aligned} \eta_{passive} = & \frac{8\pi \cdot A_1 L_1}{V_M} \left[\frac{(L_1 + L_2)}{(R_{Leq1} + R_{Leq2})^2 + (L_1 + L_2)^2 (2\pi f_L)^2} \right] \\ & \times \left[R_{L1} - L_1 \cdot \frac{(R_{Leq1} + R_{Leq2})}{(L_1 + L_2)} \right] \left[1 + e^{-T_L \cdot \frac{(R_{Leq1} + R_{Leq2})}{2(L_1 + L_2)}} \right] \\ & + \frac{1}{V_M} \left[V_M + A_1 L_1 \cdot 2\pi f_L - B_1 R_{Leq1} \right] \end{aligned} \quad (B.18)$$

Let $\tau_L = \frac{(L_1+L_2)}{(R_{Leq1}+R_{Leq2})}$ and $\omega_L = \frac{2\pi}{T_L}$, the efficiency in passive power sharing can be described as

$$\begin{aligned} \eta_{passive} = & \frac{8\pi \cdot L_1}{R_e} \frac{\omega_L \tau_L}{(R_{Leq1}+R_{Leq2})} \left[1 + e^{-\frac{\tau_L}{2\tau_L}} \right] \\ & \times \left[\frac{L_2 \tau_L \cdot R_{Leq1} - \tau_L^2 R_{Leq2} R_{Leq1} - L_1 L_2 + \tau_L \cdot R_{Leq2} L_1}{(1 + \tau_L^2 \cdot \omega_L^2)^2} \right] \\ & + 1 + \left[\frac{L_1 L_2 \cdot \omega_L^2 - \tau_L \cdot L_1 R_{Leq2} \cdot \omega_L^2 - R_{Leq1} R_{Leq2} + \tau \cdot L_2 R_{Leq1} \cdot \omega_L^2}{R_e \cdot (R_{Leq1} + R_{Leq2}) \cdot (1 + \tau_L^2 \cdot \omega_L^2)^2} \right] \end{aligned} \quad (B.19)$$

With the assumption $\omega_L \cdot \tau_L \ll 1$, and letting $R_{Leq,cm} = (R_{Leq1} + R_{Leq2})/2$ and $\Delta R_{Leq} = |R_{Leq1} - R_{Leq2}|$, the efficiency with passive power sharing is approximately

$$\eta_{passive} \approx 1 - \frac{R_{Leq,cm}}{2R_e} + \frac{\Delta R_{Leq}^2}{8R_e R_{Leq,cm}}. \quad (B.20)$$

From Eq. B.8 and Eq. B.20, it is shown that with some R_L mismatch, the passive power sharing reduces the total conduction loss compared to active power sharing approach.

B.1.3 Numerical Example of Efficiency Comparison

In active power sharing, current in each phase ($i_{L,i}$) is equal, so

$$i_{L,i}(t) = \frac{v_g(t)}{2R_e} \quad i = 1, 2. \quad (B.21)$$

By following the analysis in B.1.1 and considering the R_L and V_F effects, the duty ratio in each phase is

$$d_i(t) = \frac{\left[\frac{R_{L,i}}{2R_e} - 1 \right] v_g(t) + (V_o + V_{F,i})}{\left[V_o + V_{F,i} - \frac{R_{on,i}}{2R_e} v_g(t) \right]}. \quad (B.22)$$

The conduction loss can be calculated as

$$\begin{aligned} P_{loss,i} = & \frac{2}{T_L} \int_{t=0}^{T_L/2} \left\{ i_{L,i}(t)^2 \cdot R_{L,i} + i_{L,i}(t)^2 \cdot d_i(t) \cdot R_{on,i} \right. \\ & \left. + [1 - d_i(t)] \cdot i_{L,i}(t) \cdot V_{F,i} \right\} dt \end{aligned} \quad (B.23)$$

In passive power sharing, both phases have identical duty ratio ($d(t)$), and the sum of the inductor currents is

$$i_{L1}(t) + i_{L2}(t) = \frac{v_g(t)}{R_e}. \quad (\text{B.24})$$

Both phases are connected to the same input/output. The voltage across the inductor in each phase is

$$L_i \frac{di_{L,i}(t)}{dt} = v_g(t) - i_{L,i}(t) \cdot R_{L,i} - i_{L,i}(t) \cdot d_i(t) \cdot R_{on,i} - [1 - d_i(t)] \cdot (V_{F,i} - V_o). \quad (\text{B.25})$$

From Eq. B.24 and Eq. , the inductor current in each phase is

$$i_{L,i}(t) = C_i \cdot e^{-t \cdot \frac{R_{L1} + R_{L2} + d(t) \cdot [R_{on1} + R_{on2}]}{(L_1 + L_2)}} + A_i \cos(2\pi f_L t) + B_i \sin(2\pi f_L t) + D_i. \quad (\text{B.26})$$

where A_i , B_i , C_i , and D_i are the coefficients, which are functions of $d(t)$. An example is listed here:

$$A_1 = \frac{V_M}{R_e} \frac{2\pi f_L L_2 [R_{L1} + R_{L2} + d(t) \cdot (R_{on1} + R_{on2})]}{(2\pi f_L)^2 (L_1 + L_2)^2 [R_{L1} + R_{L2} + d(t) \cdot (R_{on1} + R_{on2})]^2} - \frac{V_M}{R_e} \frac{2\pi f_L (L_1 + L_2) [R_{L2} + d(t) \cdot R_{on2}]}{(2\pi f_L)^2 (L_1 + L_2)^2 [R_{L1} + R_{L2} + d(t) \cdot (R_{on1} + R_{on2})]^2}, \quad (\text{B.27})$$

$$B_1 = \frac{V_M}{R_e} \frac{(2\pi f_L)^2 L_2 (L_1 + L_2)}{(2\pi f_L)^2 (L_1 + L_2)^2 [R_{L1} + R_{L2} + d(t) \cdot (R_{on1} + R_{on2})]^2} + \frac{V_M}{R_e} \frac{[R_{L1} + R_{L2} + d(t) \cdot (R_{on1} + R_{on2})][R_{L2} + d(t) \cdot R_{on2}]}{(2\pi f_L)^2 (L_1 + L_2)^2 [R_{L1} + R_{L2} + d(t) \cdot (R_{on1} + R_{on2})]^2}, \quad (\text{B.28})$$

$$C_1 = -A_1 - D_1, \quad (\text{B.29})$$

$$D_1 = \frac{-[1 - d(t)](V_{F1} - V_{F2})}{[R_{L1} + R_{L2} + d(t) \cdot (R_{on1} + R_{on2})]}. \quad (\text{B.30})$$

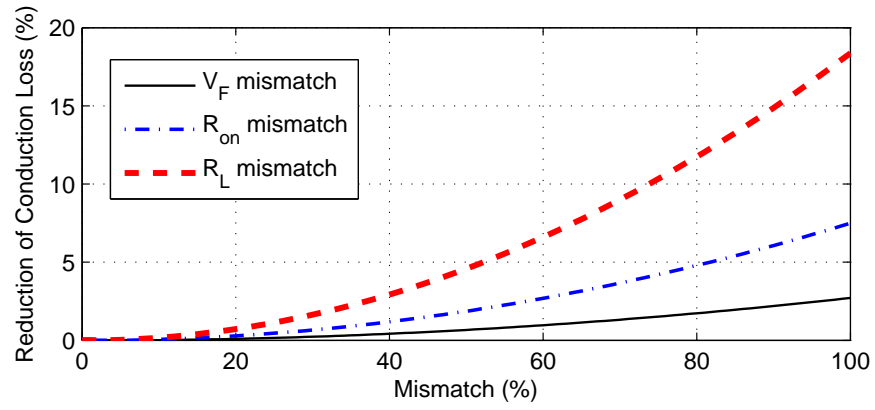


Figure B.5: Reduction of conduction loss using passive power sharing in the two-phase boost PFC rectifier (numerical example: $v_{g-rms} = 115\text{ V}$; $L = 0.3\text{ mH}$; $R_{on} \approx 0.1\ \Omega$; $R_L \approx 0.08\ \Omega$; $V_F \approx 1\text{ V}$; 600 W).

From $i_{L,i}(t)$ and Eq. B.1.3, $d(t)$ can be solved numerically. By applying Eq. B.23, the power loss in active power sharing and passive power sharing can be compared. The reduction of conduction loss can be plotted with different types of mismatches, as illustrated in Fig. B.5. The numerical example shows how the reduction in conduction losses depends on different types of mismatches.

B.2 Current Mismatch in Passive Power Sharing

Passive power sharing processes the current in each phase to be inversely proportional to the impedance, including the inductor (L) and the conduction loss resistance (R_{Leq}). If there are some impedance mismatches between the phases, there are some current mismatches between the phases. In addition, phase interleaving may also causes some current mismatch. Details of the analysis are shown in this section, including component mismatch effects in Sec. B.2.1, and phase interleaving effects in Sec. B.2.2.

B.2.1 Current Mismatch Due to Component Mismatches

Based on the averaged switch model shown in Fig. B.4, inductor current can be expressed as a first order differential equation (Eq. B.12). Using the passive power sharing, inductor current in each phase can be expressed as

$$\langle i_{L1}(t) \rangle_{T_s} = -A_1 \left(e^{-t \cdot \frac{R_{Leq1} + R_{Leq2}}{L_1 + L_2}} \right) + [A_1 \cos(2\pi f_L t) + B_1 \sin(2\pi f_L t)], \quad (\text{B.31})$$

$$\langle i_{L2}(t) \rangle_{T_s} = -A_2 \left(e^{-t \cdot \frac{R_{Leq1} + R_{Leq2}}{L_1 + L_2}} \right) + [A_2 \cos(2\pi f_L t) + B_2 \sin(2\pi f_L t)], \quad (\text{B.32})$$

where

$$A_1 = \frac{2\pi f_L \cdot V_M}{R_e} \frac{[(R_{Leq1} + R_{Leq2}) \cdot L_2 - (L_1 + L_2) \cdot R_{Leq2}]}{[(L_1 + L_2)^2 (2\pi f_L)^2 + (R_{Leq1} + R_{Leq2})^2]}, \quad (\text{B.33})$$

$$B_1 = \frac{V_M}{R_e} \frac{[(R_{Leq1} + R_{Leq2}) \cdot R_{Leq2} + (L_1 + L_2) \cdot (2\pi f_L)^2 \cdot L_2]}{[(L_1 + L_2)^2 (2\pi f_L)^2 + (R_{Leq1} + R_{Leq2})^2]}, \quad (\text{B.34})$$

$$A_2 = \frac{2\pi f_L V_M}{R_e} \frac{[(R_{Leq1} + R_{Leq2}) \cdot L_1 - (L_1 + L_2) \cdot R_{Leq1}]}{[(L_1 + L_2)^2 (2\pi f_L)^2 + (R_{Leq1} + R_{Leq2})^2]}, \quad (\text{B.35})$$

$$B_2 = \frac{V_M}{R_e} \frac{[(R_{Leq1} + R_{Leq2}) \cdot R_{Leq1} + (L_1 + L_2) \cdot (2\pi f_L)^2 \cdot L_1]}{[(L_1 + L_2)^2 (2\pi f_L)^2 + (R_{Leq1} + R_{Leq2})^2]}. \quad (\text{B.36})$$

Let $\tau_L = \frac{(L_1 + L_2)}{(R_{Leq1} + R_{Leq2})}$ and $\omega_L = \frac{2\pi}{T_L}$, the current mismatch in passive power sharing can be written as

$$\begin{aligned} \langle i_{L1}(t) \rangle_{T_s} - \langle i_{L2}(t) \rangle_{T_s} &= -(A_1 - A_2) \cdot \left(e^{-\frac{t}{\tau_L}} \right) \\ &\quad + (A_1 - A_2) \cdot \cos(\omega_L t) + (B_1 - B_2) \cdot \sin(\omega_L t) \end{aligned} \quad (\text{B.37})$$

Let $L_{cm} = (L_1 + L_2)/2$ and $\Delta L = |L_1 - L_2|$. Eq. B.37 can be re-written as

$$\begin{aligned} \langle i_{L1}(t) \rangle_{T_s} - \langle i_{L2}(t) \rangle_{T_s} &= \frac{V_M}{R_e} \cdot \frac{1}{2R_{Leq,cm}} \cdot \frac{1}{(1 + \tau_L^2 \omega_L^2)} \\ &\quad \times \left\{ (\tau_L \omega_L \cdot \Delta R_{Leq} - \omega_L \cdot \Delta L) \left[\cos(\omega_L t) - e^{-\frac{t}{\tau_L}} \right] \right. \\ &\quad \left. + (-\tau_L \omega_L^2 \cdot \Delta L - \Delta R_{Leq}) \cdot \sin(\omega_L t) \right\} \end{aligned} \quad (\text{B.38})$$

$$\begin{aligned} \langle i_{L1}(t) \rangle_{T_s} - \langle i_{L2}(t) \rangle_{T_s} &= \frac{V_M}{2R_e} \cdot \frac{1}{(1 + \tau_L^2 \omega_L^2)} \times \left\{ \frac{\Delta R_{Leq}}{R_{Leq,cm}} \cdot [\tau_L \omega_L \cdot \cos(\omega_L t)] \right. \\ &\quad - \frac{\Delta R_{Leq}}{R_{Leq,cm}} \cdot \left[\tau_L \omega_L \cdot \left(e^{-\frac{t}{\tau_L}} \right) + \sin(\omega_L t) \right] \\ &\quad + \frac{\Delta L}{L_{cm}} \cdot \left[\tau_L \omega_L \cdot \cos(\omega_L t) + \tau_L \omega_L \cdot \left(e^{-\frac{t}{\tau_L}} \right) \right] \\ &\quad \left. - \frac{\Delta L}{L_{cm}} \cdot [\tau_L^2 \omega_L^2 \sin(\omega_L t)] \right\} \end{aligned} \quad (\text{B.39})$$

Based on the assumption made in the previous section, $\omega_L \cdot \tau_L \ll 1$, and considering the R_{Leq} mismatch only, maximum inductor current mismatch can be written as

$$\max[\Delta i_L] \approx \frac{V_M}{2R_e} \cdot \frac{\Delta R_{Leq}}{R_{Leq,cm}}. \quad (\text{B.40})$$

By considering the L mismatch only, maximum inductor current mismatch can be written as

$$\max[\Delta i_L] \approx \frac{V_M}{2R_e} \cdot (\tau_L \omega_L) \cdot \frac{\Delta L}{L_{cm}}. \quad (\text{B.41})$$

From Eq. B.40 and Eq. B.41, based on the assumption $\omega_L \cdot \tau_L \ll 1$, the maximum current mismatch due to the inductor mismatch is much smaller than the mismatch due to R_{Leq} mismatch.

B.2.2 Current Mismatch Due to Phase Interleaving

Current mismatch is not only affected by the component mismatch, but also by the phase shift. To analyze the phase interleaving effect in current mismatch, an s-domain current loop model is constructed, as shown in Fig B.6. The difference between master and slave phases is the phase delay function ($G_d(s)$) in the gate drive signal. The rest of the current loop blocks are the same in each phase, including current controller ($G_c(s)$), input voltage to inductor current dynamics ($G_{ig}(s)$), duty ratio to inductor current dynamics ($G_{id}(s)$), and the emulated resistance (R_e) modeled as the relationship between the input voltage (v_g) to the total inductor reference current (i_{ref}).

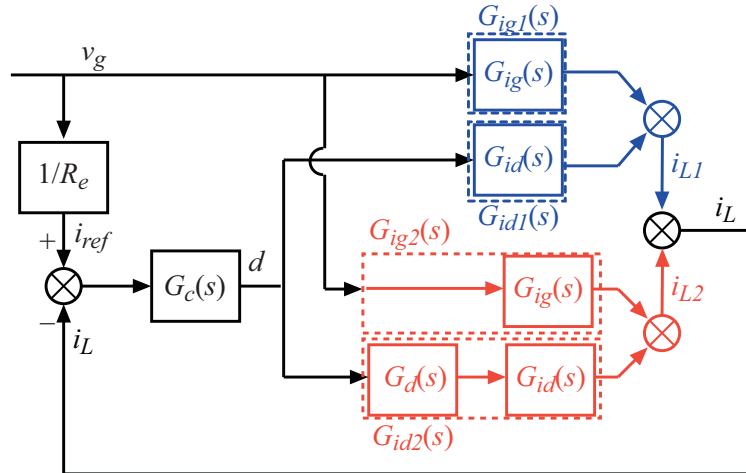


Figure B.6: Two-phase interleaved PFC rectifier model, including phase shift modeled by $G_d(s)$.

Although input voltage (v_g) of the boost PFC rectifiers is a time varying signal, the averaged

switch model shown in Fig. B.4 is a linear system. Therefore, s-domain current loop model can help to study the current mismatch due to the phase shift.

Based on the model in Fig. B.6, inductor current in each phase can be expressed as a function of v_g , as

$$i_{L1}(s) = \frac{v_g(s)}{R_e} \cdot \left(\frac{G_c(s) \cdot R_e}{1 + G_{id}(s)G_c(s)[1 + G_d(s)]} \right) \times \left[\frac{G_{ig}(s)}{G_c(s)} + \frac{G_d \cdot G_{id}(s)}{R_e} + G_{id}(s)G_{ig}(s)(1 - G_d(s)) \right]. \quad (\text{B.42})$$

$$i_{L2}(s) = \frac{v_g(s)}{R_e} \cdot \left(\frac{G_c(s) \cdot R_e}{1 + G_{id}(s)G_c(s)[1 + G_d(s)]} \right) \times \left[\frac{G_{ig}(s)}{G_c(s)} + \frac{G_{id}(s)}{R_e} - G_{id}(s)G_{ig}(s)(1 - G_d(s)) \right]. \quad (\text{B.43})$$

The current mismatch is

$$\Delta i_L(s) = \frac{v_g(s)}{R_e} \cdot \left[\frac{(G_d(s) - 1) \cdot (2G_{ig}(s) \cdot R_e - 1)}{\frac{1}{G_{id}(s) \cdot G_c(s)} + (1 + G_d(s))} \right]. \quad (\text{B.44})$$

Eq. B.44 shows that the current mismatch is affected by the input voltage dynamics and by the phase shift between the master and the slave phases.

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